Analysis and characterization of substrate and connection couplings in 3D circuits : Towards compact models

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Analyse et Caractérisation des Couplages Substrat et de la Connectique dans les Circuits 3D; vers des Modèles Compacts

(Analysis and characterization of substrate and connection couplings in 3D circuits; towards compact models)

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To my familly
献给我的家人、董媛

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1 General Introduction

The electronics industry has been the largest industry since 1996 and had reached about 1.5 trillion dollars by 2010[1, 2]. The proposal of doubling the number of transistors on an integrated circuit (IC) chip every 24 months by Gordon Moore in 1965 (the so-called Moore's law[3]) has been the most powerful driver for the emphasis of the microelectronics industry in the past 50 years[4]. This law enhances lithography scaling and integration, in two-dimensions (2D), of all functions on a single chip. The exemplifications of these integrated technologies are Systems-on-Chip(SoC)[5] and Systems-in-Package (SiP)[6].

As consequence of requirement of higher clock frequencies and lower power consumptions, nowadays, these conventional 2D planar technologies begin to face challenges from technological and financial points of view: physical limits, processing complexity, fabrication costs etc. These strong increase of the quantitative and qualitative number of features, required for the current and future multimedia or mobile applications, are exponentially increasing the design complexity. "Continued technology scaling together with the integration of disparate technologies in a single chip means that device performance continues to outstrip interconnect and packaging capabilities, and hence there exist many difficult engineering challenges, most notably in power management, noise isolation, and intra and inter-chip communication."[7] Interconnect line delays also become an obstacle in 2D Very-large-scale integration (VLSI) systems relative to power dissipation, delays in transistor switching etc. Consequently, technological approaches other than scaling are promptly investigated to continue following or getting over Moore's Law.

1.1 From Two-Dimension to Three-Dimension

Novel three-dimensional (3D) integration technology with smaller form factors, higher integration density and the support for the mixed-technology chips, appears to be the most promising candidate. [8]-[9] It is emerged as an effective way to improves performance.[10] Compared with 2D classical schemes, 3D integration potential benefits are numerous, such as performance improvement and flexible heterogeneous system combinations (logic Complementary Metal-Oxide-Semiconductor(CMOS), Radio Frequency (RF) analog function, memories). Stacking ICs vertically enables the significant shortening of the interconnect line networks (Figure 1-1), thereby decreasing interconnect line delays, which become a significant obstacle in 2D VLSI systems relative to delays in transistor switching, and the power dissipation while increasing the integration density, leading to smaller form factors and reduced fabrication costs [11, 12].

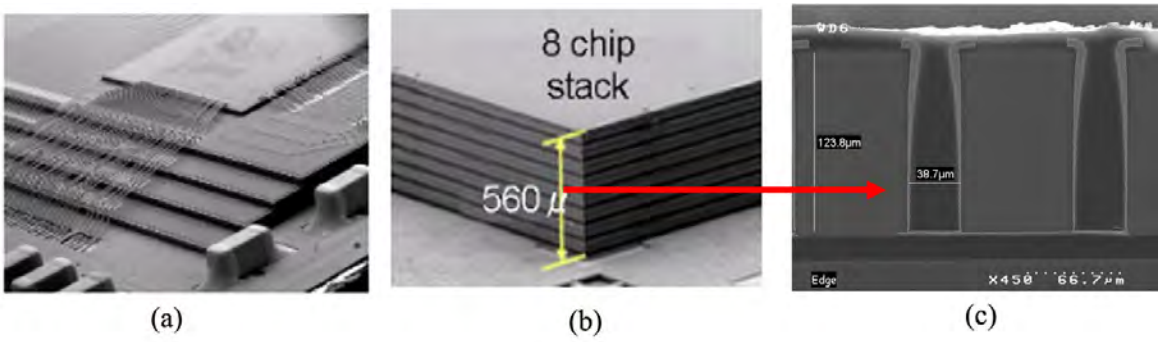


Figure 1-1 (a) Stacked chips with wire bonding. (b) 3D TSV stacking structure (Source: SAMSUNG). (c) Cross-section view of 3D TSV stacking structure. (Source: CEA-LETI)

Currently, using mature, controlled micro and nano technologies, 3D integrated systems can be obtained by stacking vertically 2D integrated circuits using wire-bonding.(Figure 1-2) But wire-bonding only enables the connecting of chip input/output pads located at their perimeter. Moreover, wire-bonding presents disadvantages in terms of surface and propagation delays depending on the application frequency clock and the wire-bond lengths (Figure 1-1(a)). As consequence, new 3D integration technologies are needed. Generally speaking, 3D integration consists of 3D IC packaging, 3D IC integration, and 3D Si integration.[4, 13]

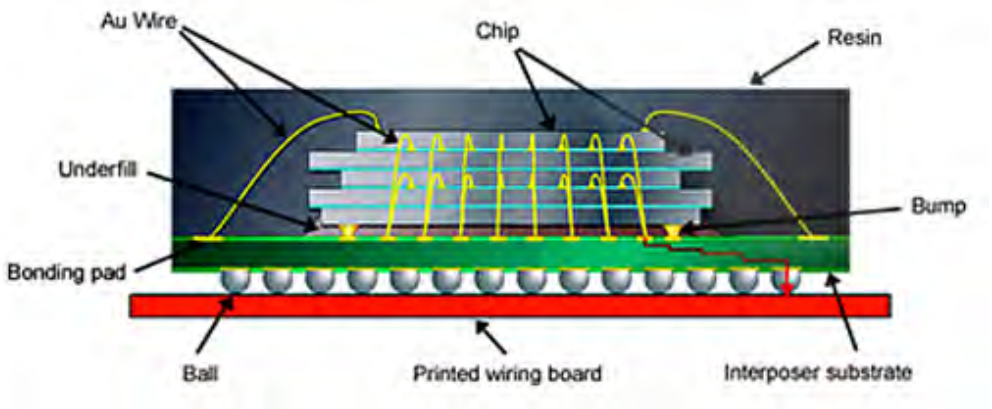


Figure 1-2 Example of SiP structure (SiP technology of 5 stacked chips) (Source: Renesas[14])

3D technology is faced to many technological challenges, like completion of vertical interconnects which ensure the signal transmission, bonding with alignment of functional dies and substrate thinning[12].

Through-silicon via (TSV) comes to our view and makes 3D IC to be more realizable. Actually, William Shockley had invented TSVs more than 50 years ago [15, 16], but at that time, it was not intended for 3D Si/IC integration. Now it plays an important role in 3D IC/Si integrations; it separates 3D IC packaging from 3D IC/Si integrations, since the latter two apply TSV, but 3D IC packaging does not. There are also difference between 3D IC and 3D Si integrations[17]. 3D IC integration is stacking chips with bumps while 3D Si integration is stacking wafers without bumps (i.e., bumpless).[18]

An example of a 3D TSV stacking with three ICs is shown in Figure 1-3. The electrical connections are ensured by innovative pre- or post-processed metallic structures: redistribution layers (RDL), copper pillars and TSV. Top, backside redistribution lines and different density TSV allow building dense and complex 3D interconnection structures by mechanically and electrically linking different stacked classical ICs. The RDL is used to distribute power and high speed signals on die top or backside surfaces and TSV is a key

enabling technology for 3D integration, propagating signals through systems silicon layers. Solder balls are put on the 3D systems' bottom layers' backsides to ensure connection with their environment.

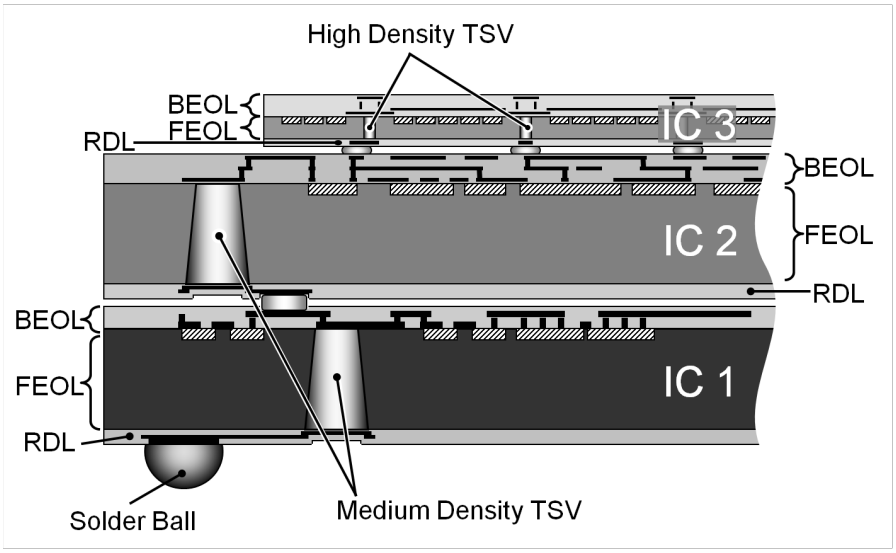


Figure 1-3 Example of vertical/3-D stacking with three ICs

The 3D integration enables the integration of different types of chips and devices in a single package (Figure 1-4), or a compact subsystem providing a maximum benefit from highly specialized and heterogeneous technologies. However, in order to take full advantage of the 3D IC, the decision must come upfront in the architecture planning process rather than as a packaging decision after circuit design is complete[19]. This requires taking 3D design space into account, right from the start of the system design, in order to distribute its different parts into a new set of chips that will be stacked. While it puts forward the new challenge to the designer due to the high density integration and its emerging technology status, notably in properly characterizing and electrically modeling the 3D interconnects.

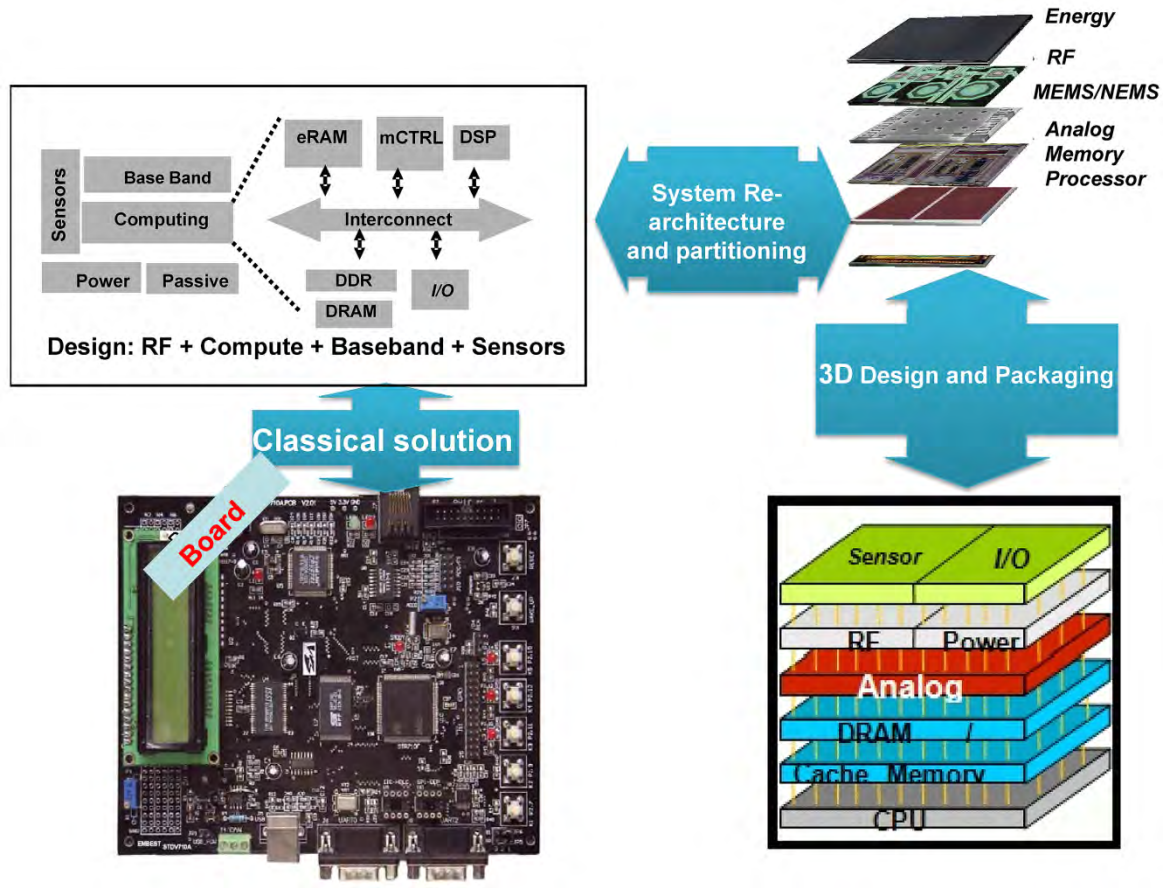


Figure 1-4 Classical 2D solution versus 3D concept

1.2 Roadmap of 3D Integrated Circuits

3D TSV device gives a bright way of the development of electronics industry. Actual forecasts are from 7 to 16 millions of 3D TSV wafers to be shipped by 2016[20]. 3D integrated circuits, where interconnections are made at global or intermediate levels of the chip by TSV, allow better integration, bandwidth and electrical performances by reducing signal delays, smaller form factor and pin count, and overall a better packing density. In this type of technology, the most common solutions use stacked memory devices [21-24], but also sensors including CMOS (imaging) sensors [25-29] bonded with DSP (Digital Signal Processing). Future applications aim at packing multi-core processors, caches and memory hierarchy and other incompatible technologies in a heterogeneous integration solution. Figure 1-5 shows a roadmap of the 3D-IC TSV.

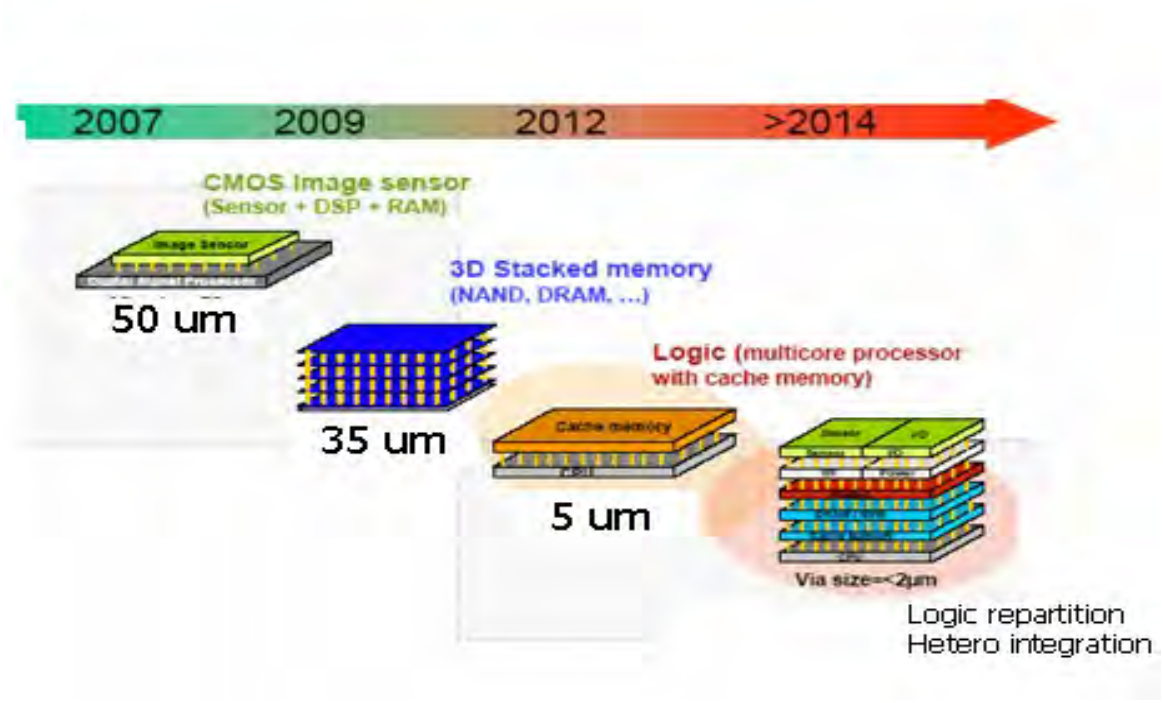
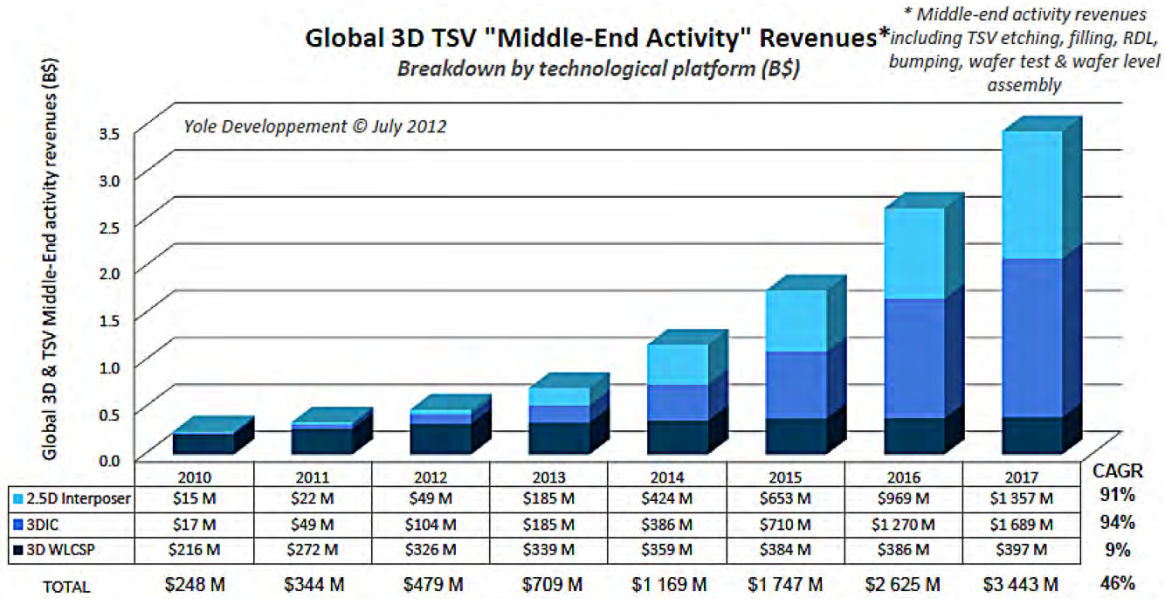


Figure 1-5 3D-IC Roadmap (Source: STMicroelectronics/LETI)

According to the report from Yole Development(Figure 1-6), 3D TSV device market will reach $38B value in 2017 (9% of the total semiconductor products), growing more than 10 times faster than global semiconductor industry.[30]



	2010	2011	2012	2013	2014	2015	2016	2017	CAGR
2.5D Interposer	$15 M	$22 M	$49 M	$185 M	$424 M	$653 M	$969 M	$1 357 M	91%
3DIC	$17 M	$49 M	$104 M	$185 M	$386 M	$710 M	$1 270 M	$1 689 M	94%
3D WLCSP	$216 M	$272 M	$326 M	$339 M	$359 M	$384 M	$386 M	$397 M	9%
TOTAL	$248 M	$344 M	$479 M	$709 M	$1 169 M	$1 747 M	$2 625 M	$3 443 M	46%

Figure 1-6 Global 3D TSV “Middle-End Activity” Revenues (Source: Yole Development) [30]

The application of TSV technology has been used in realistic products. In this year (2013), the Hybrid Memory Cube (HMC) Consortium[24] just published HMC Specification 1.0. With eight links, a memory cube can reach a peak 320GB/s of aggregate bandwidth. That means it offers up to 15 times the performance of DDR3 (Double Data Rate type three) [31]memory, while using 70% less energy.

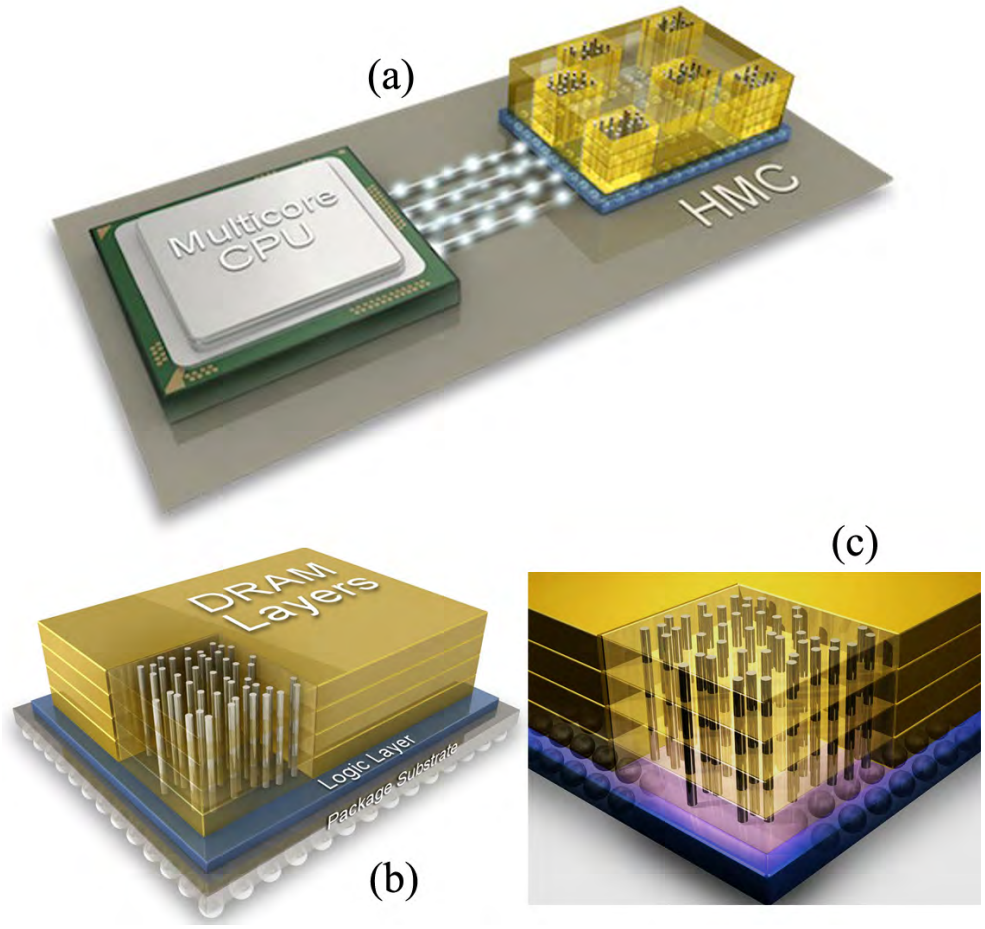


Figure 1-7 Hybrid Memory Cube memory architecture used TSVs ([24])

Due to the technology report[21-23], the Hybrid Memory Cube is essentially a stack of up to eight DRAM (Dynamic Random Access Memory) memory dies, connected to each other with TSVs, sitting atop logic and switching layers that controls input and output to all eight dies (c.f. Figure 1-7). From the view of HMC Consortium, “Hybrid Memory Cube is a revolutionary innovation in DRAM memory architecture that sets a new standard for memory performance, power consumption and cost.”[24] Figure 1-7 (c) shows the structure of TSVs used in HMC.

Actually, the 3D TSV applications range is wider and the pure memories applications are no more the main ones. For example, it has been applied to the CMOS image sensors contributing to decrease the thickness and dimensions of image sensor while increase pixels density.

CMOS image sensors using a "via last" approach with via diameters of about 50μm and similar silicon thicknesses have been already introduced in the market. [32] Figure 1-8 shows a novel 3-D image processor which used TSV to incorporate an image sensor, A/D converter, frame memory and reconfigurable image processor in a four-layer stacked configuration. [33]

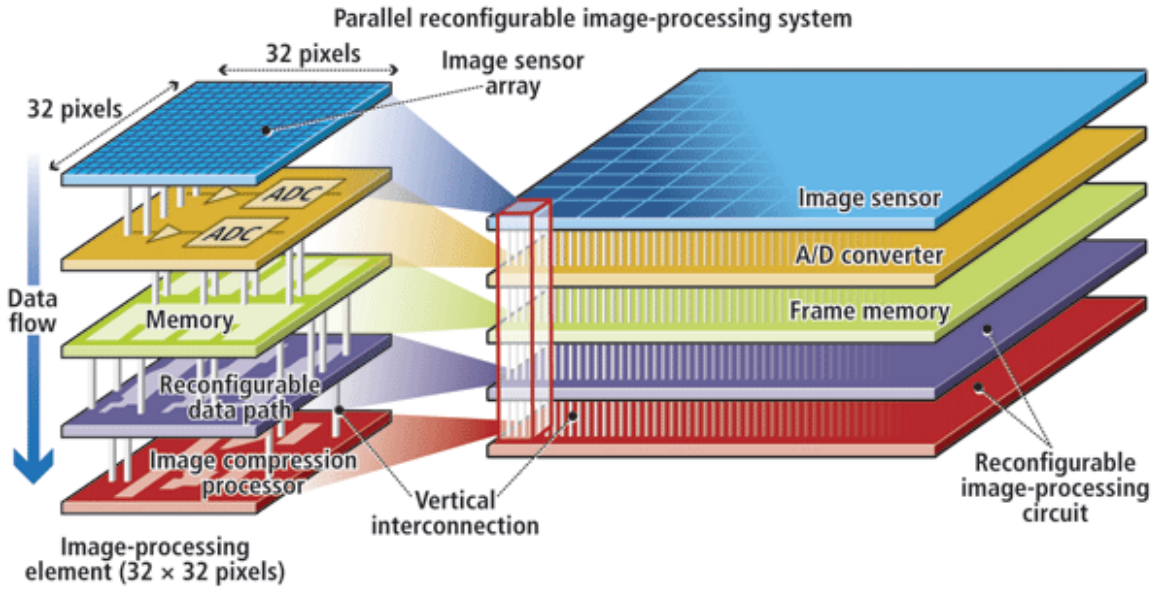


Figure 1-8 A novel 3-D image processor used TSV technology that incorporates an image sensor, A/D converter, frame memory, and reconfigurable image processor in a four-layer stacked configuration. (Source: vision-systems)

In Figure 1-9, a forecast of 3D integration products by 2017 from Yole development is shown[30]. From the figure one can see that, by 2017, the 3D integration products will be found almost in every part of electronics field. And the mobile phone will take 42% of the all the 3D integration products due to its demand of portability which greatly benefited from the 3D technology.

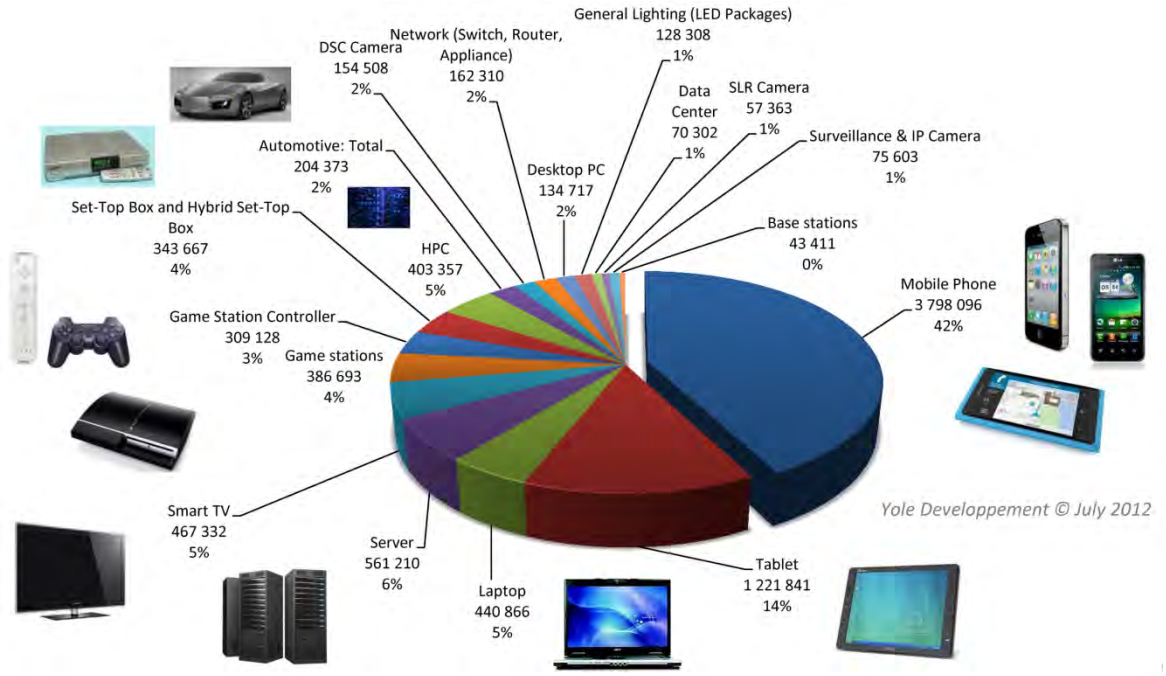


Figure 1-9 3D Integration Production Forecast by 2017 (All 3DTSV Platforms) (Source: Yole Development)[30]

1.3 Outline

First of all, in chapter 1, the introduction is a state of the art in 3D integrated circuit. We state 3D architectures for IC integration are a promising alternative to standard 2D designs, when increasing interconnect densities and rising cost of (IC) manufacturing.

Chapter 2 presents some background knowledge on 3D ICs and substrate noise. The challenge encountered in 3D and the fabrication technologies of TSV are also investigated. Classical methods for substrate noise analysis on analog devices are introduced.

In chapter 3, we propose a new substrate network extraction technique, relying on the Transmission Line Matrix and the Green kernels, for 3D circuits. The substrate coupling and loss in Integrated Circuits can be analyzed by these algorithms. This technique could be used to metal contacts or/and Through Silicon Vias (TSV), in any number, and they can be placed anywhere into the substrate, or onto. This feature makes it very suitable for the multi-layer substrates.

In chapter 4, 3D-Interconnects compact models is extracted and then a 3D-Transmission Line Extractor tools is developed. Modeling approach is validated through frequency analyses by comparing the S-parameters measured on the test structures with those obtained by simulating their respective equivalent electrical models over a wide frequency range, typically from DC to 20GHz.

In chapter 5, improved models and several future working directions concerning the research on 3-D IC are proposed. The analysis in thermal effect, skin and eddy current effect and fluctuations correlation analysis are also presented.

The chapter 6 summarizes the contributions of this dissertation work, draws conclusions of the manuscript.

2 Background Knowledge for TSV and Substrate Coupling Noise

2.1 From 2D to 3D: Opportunities and Challenges

In the last chapter, it was shown that Three-Dimensional Integrated Circuits (3D-IC) have a bright future. However even with the advantages that 3D-IC offers, there are several major challenges to the widespread adoption of 3D architectures due to high density integration and its emerging technology status, notably in properly characterizing and electrically modeling the 3D interconnects. High density integration and high system frequency also result in substrate noise coupling becoming one of the most significant considerations in the design process due to its significant impact on the performance of ICs. [34].

Thus, there will be a need for effective tools to analyze the practical layouts and to calculate the electrical performance of the circuit. The resistance, the partial capacitance matrix and the partial inductance matrix must be calculated in order to analyze the substrate coupling.

The most reliable methodology for analyzing the practical layout and calculating the electrical performance of the circuit is to solve the Maxwell equations directly[35], by utilizing the finite element and Finite Difference Time Domain (FDTD) techniques, among others. These methods can yield accurate results and have wide applicability; however their computational costs are usually prohibitively high. Particularly with regard to today's computers, the inability to solve large-scale problems in a limited time is unacceptable. It is also difficult to ensure the stability of this method.

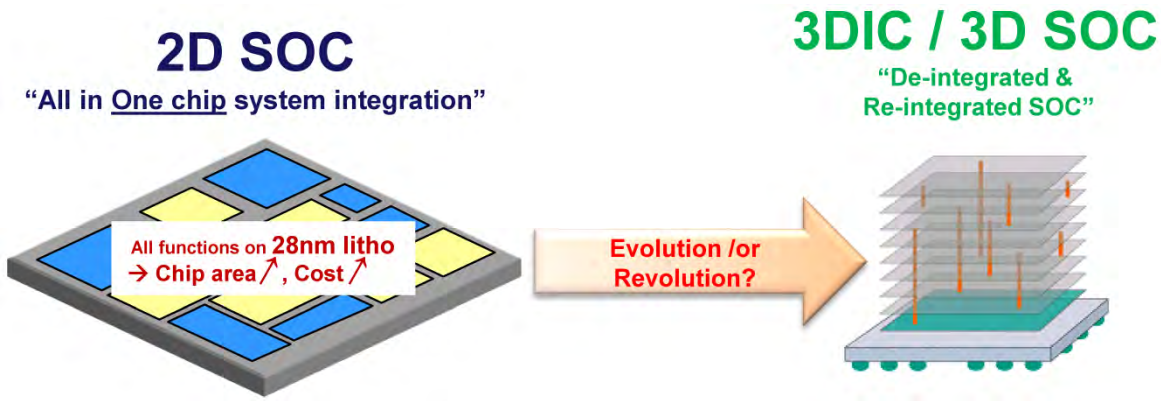


Figure 2-1 The 2D SoC vs. 3DIC[20]

In high-frequency situations, TSVs can be a major source of substrate noise, resulting in reduced device performance and increased power consumption levels. Thus, for

high-frequencies, it is important to thoroughly understand the substrate coupling characteristics in order to prevent the whole system, including the die and its packaging, from experiencing bounces, or parasitic oscillations. The extent of circuit performance degradation caused by the silicon substrate is very high. Considering the Radio Frequency (RF) range, the substrate at some nodes of interest might have a Resistance, Inductance and Capacitance (RLC) behavior, which would essentially be a Resistance and Capacitance (RC) behavior at low frequencies.

Indeed, the main difficulty in Through Silicon Via (TSV) modeling is that the 3D interconnection's overall electrical context must be completely considered. Consider modeling the current paths, for example, of an environment comprised of top or back metal redistribution lines. The parasitic coupling capacitance must be analyzed in various configurations [36], depending on whether the TSV is bounded by nearby interconnect wires located above, below or to the sides. However, the TSV model in [36] was simplified by neglecting both the TSV inductance and the oxide capacitances, and by assuming a high-resistivity substrate. Another aspect of current interconnect modeling is that many authors describe their equivalent electrical models as lumped. When considering the global electrical context at low and medium frequencies, it is true that some interconnection elements of a network can still be described as lumped while their length is smaller than a tenth of the propagation signal wavelength. However, most interconnect electrical models must be distributed into several Resistance, Inductance, Capacitance and Conductance (RLCG) elementary cells in order to properly quantify the electromagnetic effects.

As seen in the case of local metal layer interconnect line structures [37], the 3D interconnect's global environment necessitates modeling the substrate coupling effects, which at high frequencies can no longer be neglected. Electrical modeling methods are then dependant on the substrate type. Several substrate extraction techniques have been proposed in research, however, most of them cannot be employed for Systems-On-Chip (SoC) with realistic dimensions, or they are only suitable for a specific type of structure or technology process [38] [39].

Many challenges must be overcome for 3D architecture to become widely adopted.

2.1.1 The Commercial Availability CAD Tools Will be a Necessity

Commercially available CAD tools are necessary to facilitate a flexible floor plan, and for better vertical and horizontal placement and routing steps, including better thermal modeling and specific Design for Yield(DFY) constraints. Previous work has focused mainly on TSV electrical modeling as it plays a central role in achieving high-density integrated 3D systems, and because it enables a large variation in the shapes, the dimensions of the radius and length, the dielectric thickness and the filling material. Some researchers[40] have investigated the impacts of the TSV cross-section and radius on frequency responses. Y. Liang and Y. Li [34] have contributed the analytical expressions for the resistance, the self-inductance and mutual-inductance of a copper-filled, tapered, high-density TSV, which were obtained from a cylindrical conductor formula that utilized the current density. Two coupled cylindrical TSVs were studied [41] and the closed-form expressions for the self and mutual parameters were reported, however the two TSVs were isolated from their environment. The need for a 3D platform, and the problems of missing some pieces of the design, is quickly becoming a reality at the design and foundry levels, with manufacturers now putting the pieces into place for a 3D-IC design methodology. In addition to the technology issues, the Electronic Design Automation (EDA), which is at the core of 3D Silicon (Si) integration, is still far from ready[4]. The need for standards for the 3D-Si

integration industry is urgent. With standards in place for the EDA, work on the design, simulation, analysis, verification and manufacturing preparations could move forward.

2.1.2 Novel System Design Methodologies, New Design Tools and System Architecture Solutions

A major challenge will be the determination of the best trade-offs between system partitioning and costs, in considering the novel 3D integration packing approach. 3D integration technology allows the stacking of different chips and devices in a single package. The maximum benefit can be obtained through the use of heterogeneous and highly specialized technologies, and the possibility of determining the optimal partitioning early in the design process[42-47]. New system design methodologies are thus needed to handle this emerging 3D-TSV integration approach.

Computing performances can attain speeds in the order of Tera-operations per second by allowing increasing memory bandwidth, by pushing forward the miniaturization necessary for consumers' wireless mobile applications, by mastering pin counts, by utilizing Multi-core architectures (from tens to several tens of cores), and due to the capabilities provided by nanometer technologies (typically 32 nm, and beyond). However, issues related to the memory hierarchy and its throughput still remain to be resolved. The best system partitioning trade-off at the chip level, performance determinations for memory throughput, power consumption, size and form factors, and the trade-offs for technology versus the costs for on-chip and off-chip storage, should all be determined.

The crucial elements of the device, other than the computing power, are: the ability to manage heterogeneous technologies such as digital, analog, RF and discrete passive devices (resistors, inductances and capacitors), and the software. Analog and RF components do not have the same level of downscaling as do numerical devices, and even more problematically; the size of the analog and RF components can increase as the technology is scaled down.

Analog, RF and power circuits do not scale down with the processing nodes at the same rate that the digital logic does. The I/O and analog circuitries (which make up about 40 percent of the original device) only scale down at about half the rate of digital logic circuitries. An order of magnitude is lost by the dice/wafer over several process generations, due to the fact that the dice does not scale down as quickly as do the digital transistors.

Partitioning the different layers of silicon overcomes this limitation, allowing designers to utilize the best of each technology. By changing single-chip packages to 3-D devices, systems with higher transistor densities and lower power consumption levels can be achieved. The distances the data travels will be shortened, and the manufacturing costs will also decrease through die reuse generalizations.

Some hierarchical concepts for the multi-physics models include:

- The definition of a unified model interface based on a clear understanding of the properties of abstraction levels and associated modeling languages
- Models with adjustable accuracy
- Integration into the system design flow
- Circuit, reduced-order and behavioral models will be used in the simulation of subsystems or sub-problems of the demonstrators
- Simulation of data-based performance models to estimate the degree of feasibility of

the parameter set and sensitivity matrices of the set of component parameters.

This work would then enable the development of a coherent hierarchical modeling strategy in order to create a continuum of models over all relevant abstraction levels.

Based on application-specificity, the work would also be focused on high-level hierarchical system modeling. Part of the focus would be on defining the best partitioning for high-level hierarchical models, whether these models deal with thermal, electromagnetic or reliability issues. Ultimately, these models will serve as novel architectures for 3D memories, the computing will be defined, and new methods and tools will be developed for the design of 3D systems. The physical characteristics related to the packaging such as the electrical voltage, signal integrity, throughput, power consumption, thermal characteristics, size, and form factors, should also be considered.

2.1.3 Thermal concerns by increased power densities and others

Excessively high temperature can significantly degrade the reliability of the interconnection of the device, and even cause functional failures through the electro-thermal coupling [48-51]. When ICs are stacked, there are insulation layers between each IC, which will isolate the IC's from heat dissipation. Avoiding hot spots on the overlaps can also be an issue. These issues are a priority, especially for TSVs where electrical currents are concentrated. It is necessary to examine a more realistic situation in which the materials' temperature-dependent properties like resistivity and the dielectric constant are considered.[52] An analytical model of the temperature distribution in a multi-die stack with multiple heat sources was developed [51]. It showed that package and heat sink thermal resistances played a more important role in determining the temperature rise than did the thermal resistances intrinsic to multi-die stacks.

Thermo-mechanical or thermal stresses of the TSV are also now being investigated more frequently.[53-57]

2.1.4 Test and Reliability Issues for Re-partitioned Logic That Targeting New Multiple Defects Generated by the TSV and Electromagnetic Interferences

Crosstalk, propagation and radiant effects are becoming more and more important within the integrated circuit domain. Today's submicron semiconductor is operating at very high frequencies. This is particularly important for the characterization of interconnected structures that are loaded with digital circuitry and drivers. Electromagnetic Compatibility (EMC) and Signal Integrity (SI) are strongly affected by the geometry of the interconnects, and by the potentially complex nonlinear or dynamic behavior of the electronic devices collocated at the interconnect terminations [58].

There is a growing need for a great improvement in the SoC design process, in both quality and productivity.

According to the project description of CATRENE[59, 60] ,some key innovations to connect the SoC applications and design methods could be:

- *System Re-architecture Breakthrough*: Design approaches including 3D partition of geometry, technology and functional levels to facilitate the best selection of Cost/Performances trade-offs.
- *3D System Architecture Breakthrough:* Better 3D system architecture, design methods,

tools and components such as interconnects and analog and RF circuits.

- *3D Design Automation Breakthrough*: Upgrade the current design flow processes to handle 3D designs.
- *Linking the Fabrication Process to System Level Design Breakthrough*: Designing for novel silicon integration and packaging approaches to facilitate the implementation of 3D solutions, to build larger and better quality systems in less time with lower costs.

Key benefits of this 3D solution would include:

- *SoC Design Quality and Architecture Optimization.* The solutions would enable SoC designers to re-design the system architecture to achieve significantly better tradeoffs by utilizing different partitioning for the geometry, technology and functional areas
- *SoC Design Cost Reduction.* This would be achieved through a better selection of technologies to be used in each area of the system. Advanced and often expensive processes would then only be used where necesssary. The opportunity to re-use chips would also be part of the endeavor to optimize both the costs and the time-to-market.
- *Improved Flexibility and Time to Market:* The design solutions for Run Time Library (RTL) to Graphic Data System (GDS2) automation would reduce the amount of time that SoC designers must spend on largely reactive tasks, such as provisioning, configuration, testing and debugging.
- *Improved Form Factor:* Whenever possible, design concepts would facilitate a reduction in the size of the resulting product. This would also generally result in improved performances, power consumption and reliability.

When enabling high device densities in all the dimensions of a 3D integration, noise coupling and thermal effects [56, 61, 62], to which circuit performance is highly sensitive, are exacerbated. For model-based architecture designs, it is necessary to develop a means of adequately describing the impact of these effects on the performance of the blocks at each relevant abstraction level. Due to the different physical effects, to their local or global existence, and to the influence on the 3D system; different levels of abstraction must be used to decrease the simulation time, or to even make the simulation possible. These abstraction levels will vary from specific field calculations, when using differences from examples or from Finite Element methods, in order to implement behavioral models used in circuit simulations such as ELDO/SPICE, VHDL-AMS, or Verilog-AMS. This task also focuses on the development of a flexible high-level interconnect model in C++ and Java, taking into account technological data and TSV models, with the objective of enabling the estimation of the communication costs in terms of latency, throughput, power, silicon cost (based on spatial organization), and its consequent impact on functional and system performances.

2.2 The Fabrication and Integration of the Through Silicon Vias

2.2.1 New Technology and Fabrication for the Integration of Through Silicon Vias

2.2.1.1 Semiconductor Substrates

Selected technology variants for via structures, with respect to applications, will be investigated by developing and fabricating appropriate test-structures and stacks. Chemical Vapor Deposition of Tungsten (W-CVD) will be covered initially, and within the ongoing projects of Cu-CVD filling[53, 63, 64] of the TSVs etched into the silicon, aspect ratios greater than 10:1 will have to be realized. Barrier layers for the isolation of the TSVs will be examined by test-structures to determine leakage currents and break-down voltages. The wafers will be thinned for the Post Back End of Line (BEOL) Via First concept to be applied and optimized. High density interconnect modules may be examined within this work-package, giving input to the optimization of the models for the simulation of advanced packaging modules for the design flow. The work must be adjusted to be very similar to the simulation and modeling work.

Capacitive and conductive effects caused by thin oxide around the vias will increase inductive and resistive parasitic phenomena of the TSV. Analysis of the thermo-dynamic behavior of the TSV and the interlayer assembly, to determine the capacity, will need to be accomplished. Since the TSVs will represent the essential means of evacuating the heat generated inside the bonded dies, their thermal behavior will be explored and modeled, which will require the development of specific methods for the thermal characterization of the TSVs.

The type of silicon substrate in which the 3D interconnections are processed is an important parameter and has a strong impact on the 3D interconnection's electrical behavior. The electrical modeling methods are then dependant on the application's type of substrate. Two different types of P silicon substrates are typically used in CMOS/BiCMOS processes: uniform lightly doped substrate (>1Ω.cm) and heavily doped substrate (<1Ω.cm) with a thin lightly doped (>1Ω.cm) epitaxial layer[65]. Other semiconductor substrates are used in other micro or nano technologies and could embed the 3D interconnections. Silicon on Insulator (SOI), Micro-Electro-Mechanical Systems (MEMS), Systems technologies or Sensor technologies could each be used. The substrate conductivity incidence of the signal propagation and losses can then be studied, thanks to 3D electromagnetic simulators, in order to validate other results and to build electrical models.

2.2.1.2 Metal Redistribution Lines

In all 3D interconnection technology proposals, classical and mature wiring processes are widely used. The processed wires allow the distribution signals and power over the 2D surfaces of each stacked integrated circuit. In this way, BEOL processes can be reused in new 3D technologies by redistributing signals on top of the dies. Depending on the microelectronic technology, BEOL interconnections are made of aluminum or copper wires, with a thickness and resolution under one micron. Other wiring processes can also be useful in 2D signal redistribution, such as Wafer Level Packaging (WLP) processes on the top or the backside of stacked dies. Those processes use thicker (greater than 1 µm) copper or aluminum wiring, with a lower resolution; typically over ten microns. The Post-BEOL metal layers are useful in

distributing power or high speed signals on the die top or back surfaces, thanks to their thick, and high conductivity metal layers. All those metal redistribution lines are obviously isolated from the semiconductor substrate with grown dielectric layers of different thicknesses, depending on the technologies employed.

2.2.1.3 Through Silicon Vias

Typically, two different TSV technologies may be addressed and studied: medium density and high density TSV technologies.

A *medium* density TSV can be defined as a large copper tubular conical structure, isolated from the silicon substrate with grown silicon oxide around it. The external diameter varies from 50 to 60 µm, ± 10 µm, and the inside diameter varies from 40 to 60 µm. They grow through a roughly 100 µm thick silicon substrate.

A *high* density TSV can be defined as small copper bars isolated from the common silicon substrate by a thin silicon oxide film. Their width varies from 2 to 4 µm and they grow through a thinned silicon substrate of approximately 10 µm thickness. They are also obtained by the Via Last approach process.

Wafer stacks that include 2-3 µm wide, high density TSVs (~104 TSV/mm²) can be processed according to the Via Last approach. A top wafer is bonded face to face to a second one, using SiO2 bonding, and thinned down to 15 µm prior to the Via processing, as shown in Figure 2-2. The complete process flow for 3D chip stacking is divided into three main steps: wafer bonding, substrate thinning, and TSV integration.

TSV processing varies from one to one, but generally can be generalized to 3 steps: TSV patterning and filling, wafer bonding and wafer thinning.

a) Wafer Bonding [63, 66-68]

Wafer bonding applies to the three types of die to wafer, die to die and wafer to wafer bonding. The bonding technologies consist of oxide bonding, metal-to-metal bonding and polymer-adhesive bonding.

The aim of oxide bonding technique is to achieve a glue free assembling without strain at room temperature. Before bonding, SiO_2 surface is prepared with Chemical & Mechanical Polishing (CMP) and cleaning. Then, wafers are face to face bonded using direct oxide bonding technique. Perfect bonding quality can be obtained at a low temperature compatible with copper back-end of line on wafers having relatively high incoming surface topography. Finally, the stacking is stabilized by an annealing step at toughly 500°C under N_2 atmosphere

b) Wafer thinning [69-72]

After bonding, the backside of the top wafer is thinned down to 10-15 µm using grinding and CMP. A specific edge-outlining step is introduced to remove damages at the wafer edge, within a 3 mm ring. Figure 2-2 shows resulting two strata-3D stacks with 15 µm thick Si. The Total Thickness Variation (TTV) after thinning is about 1 µm. Surface roughness is 0.5 nm Root Mean Squared (RMS) and the bow is reduced to 20 µm after a stress release step utilizing Chemical Mechanical Polishing (CMP).

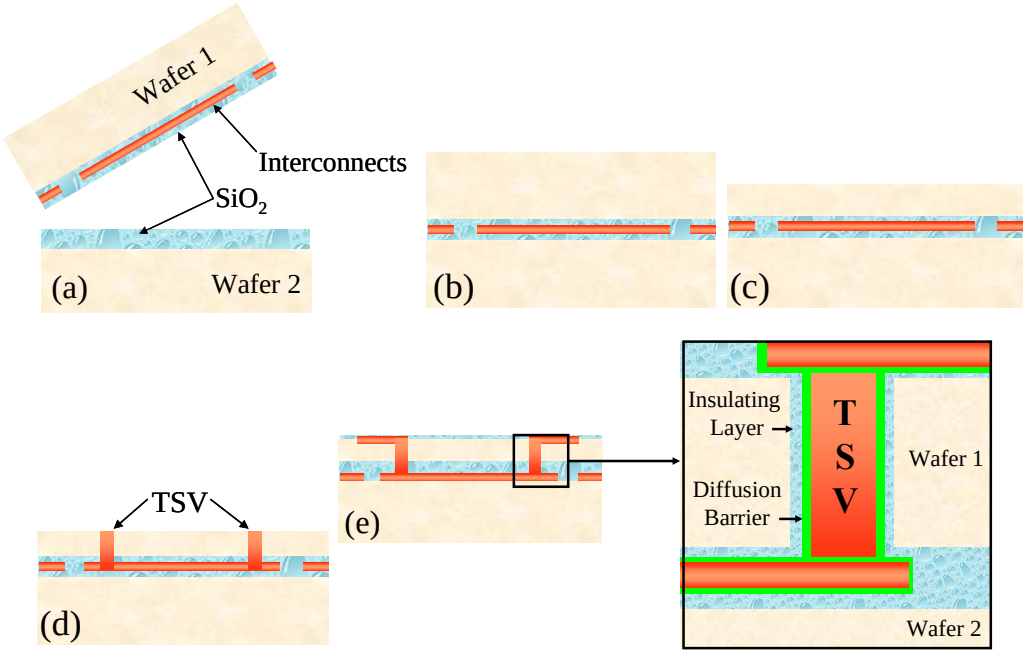


Figure 2-2 Face to Face Via Last process flow integration (a) before bonding and after bonding (b), Si thinning (c), TSV patterning and filling (d), top interconnects integration (e) (source: LHAC)

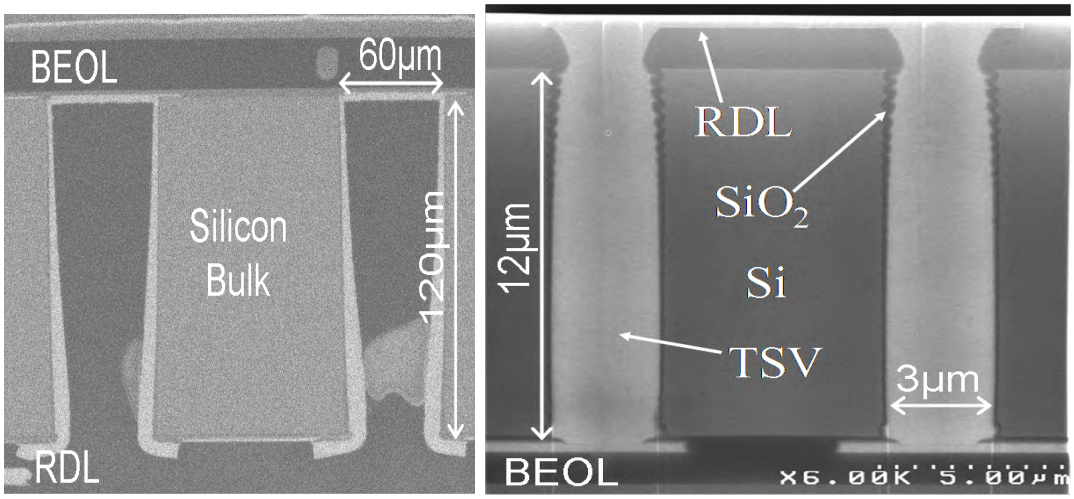
Vertical system integrations based on high (in the 1,000 range) density TSV interconnections are needed. Fabricated 200 mm wafers, with predefined regions for etching the TSVs will be processed by a combined etch process sequence for the Inter-Metal-Dielectrics (IMD) and a subsequent deep Reactive Ion Etching (RIE) into the silicon. The high aspect ratio TSVs will be isolated by low temperature oxide deposition and filled by CVD metallization, (W or Cu).

Subsequent processing for rewiring the feed-through to the metal-pads will be done by standard aluminum PVD (Physical Vapor Deposition) processes. A suitable handling concept such as gluing the supporting wafers or the use of a silicon-based electrostatic chuck will be selected for thinning the TSV-wafer and baring the TSVs from the backside. With respect to the application, the wafer will be prepared for stacking by an additional rewiring on the backside and by electroplating the metal system with Cu, Cu and Sn, or more complicated compounds. The corresponding chip or wafer for stacking the complete system will also be processed by applying aluminum rewiring and preparing the stack formation according to the overall planarity of the supplied wafer. A Chip-to-Wafer (C2W) or a Chip-to-Chip stacking (C2C) concept with respect to the Known Good Dies (KGD) and the stack formation will be applied by using appropriate assembly tools with high accuracy. The stack formation can be accomplished either by a Solid-Liquid Inter-Diffusion process (SLID) or by Micro-Bump Technology, if necessary.

c) TSV Patterning and Filling

2 and 3 µm wide and 15µm deep copper TSVs are integrated to achieve high density 3D integration, once the bonding and thinning are completed [45] First, lithography with a thick resist of about 3.5 µm is performed, before deep Reactive Ion Etching (RIE)[73] for silicon etching. Good etching profile is required for metallization, enabling integrity and good step coverage. Low undercut ($\leqslant$ 30 nm) and scalloping ($\leqslant$ 50 nm) are observed after cleaning and resist stripping that is compatible with further filling process steps. After CVD deposition of a 200 nm thick SiO2 layer on the sidewall of the TSV for isolation, a metallization is performed by successive depositions of Metal Organic (MO) CVD TiN of 20 nm, as a diffusion barrier, 50 nm PVD Cu seed featuring good adhesion for the sidewall oxide, 150 nm

conformal CVD Cu seed and an Electro Chemical Deposit (ECD) Cu filling. Specific ECD chemistries and process parameters are selected to obtain voidless filling. Figure 2-3(b) shows a Focused Ion Beam Scanning Electron Microscope (FIB SEM) cross section of a 12 µm deep and 3 µm wide TSV, after copper filling. To connect the TSVs, a top interconnect level is needed, referred to as a Re-Distribution Layer (RDL), using a conventional damascene process. After the complete integration the SiO2 bonding interface will be free of defects.



(a) (b)

Figure 2-3 FIB-SEM cross section of TSVs after filling

2.2.2 3D Interconnections [74-76].

Top and backside redistribution lines and different densities of TSV allow the building of dense and complex 3D interconnection structures, that mechanically and electrically link different stacked classical ICs to obtain a complex and dense integrated 3D application. To thoroughly understand electrical modeling issues involved in such complex interconnections, an example of a realistic 3D interconnection in a 3D IC context has been described and is illustrated in Figure 1-3. The example is of a stack of three separate 2D ICs, using medium or high density TSVs, connected by backside metal redistribution.

Solder balls are put on the bottom layer of the backside of the 3D system, to ensure connections to the world. Metal redistribution lines facilitate reaching medium density TSVs that distribute signals and power to the top side of the bottom die. Signals and power lines feed and go through the second layer by using the same kind of 3D interconnection structures. The two different types of signal propagation lines on silicon substrate that are addressed are microstrip line structures [77] , commonly used to propagate electrical signals, and Co-Planar Waveguide (CPW) transmission lines, used to propagate high frequency signals. The top die is very thin in order to connect to the rest of the 3D system by using high density TSVs. 3D interconnections can use very complex metal pathways, through different layered media, with different electrical characteristics, such as semiconductor layers, isolating layers and air. Evidently, all those layers impact the signal propagation between the separately stacked ICs, and can involve severe signal integrity issues, and thus reliability issues for the entire 3D system.

The first objective is to derive requirements for 3D objects, or TSVs, from industrial applications. Several end-user applications for mobile and multimedia devices, such as digital radio or digital video reception, have been investigated in order to derive realistic application requirements. Those requirements include typical connection counts, maximum resistance per

TSV, signal frequencies, and the TSV density for the greatest cost effectiveness. Based on these applications, a reference model of the 3D layers will also be defined, taking into account various parameters, such as the number of required technologies, the manufacturing yield, the environmental sensitivity, and the content and cost structure per layer.

2.3 Extraction Coupling Noise

Substrate or bulk is a solid semiconductor substance base (usually a planar one) on which other material is deposited. In solid-state electronics, it refers to a thin slice of material such as silicon, silicon dioxide, or other materials. These serve as the foundation upon which electronic devices such as transistors, diodes and especially ICs, are deposited.

The sources of substrate disturbances can be decomposed into two distinct phenomena, as was the case for most models proposed by various authors [78-80]. This phenomenon is illustrated in Figure 2-4. The first source of noise is caused by the overall substrate as it is injected into the entire surface of a digital block, and it is known as noise power. The second source is local, and is caused by the capacitive coupling of digital signals via the Metal-Oxide-Silicon (MOS) capacitors, the drain /substrate or metal/substrate, or the impact ionization in the gate of the MOS capacitors.[81]

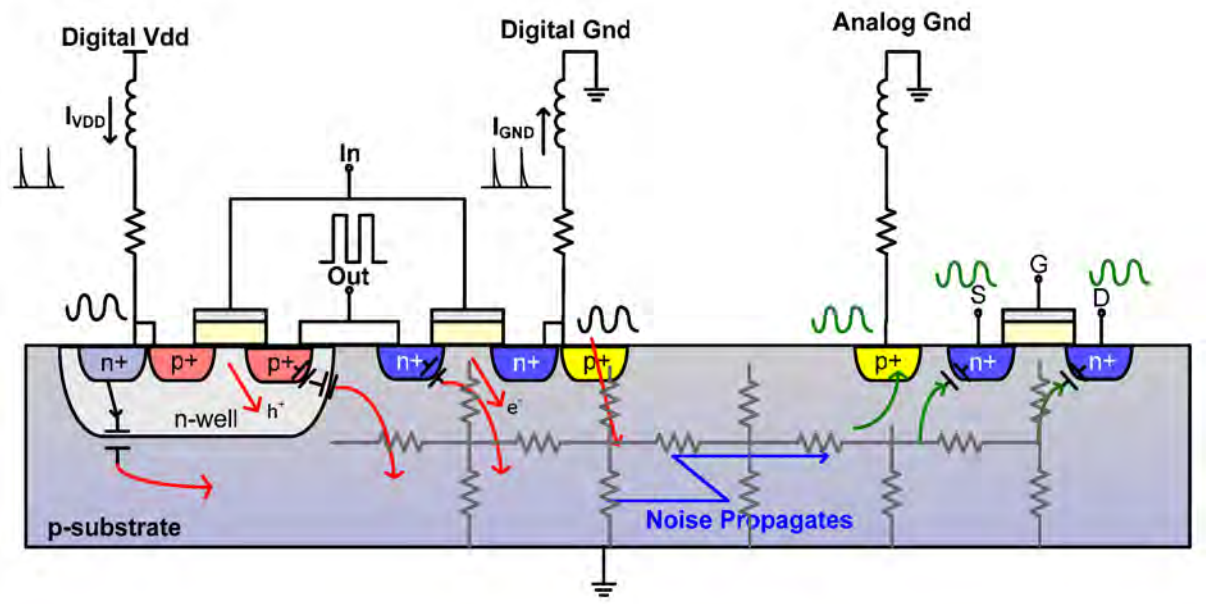


Figure 2-4 Substrate coupling in mixed-signal circuits [80]

With the rapid development of Very Large-Scale Integration (VLSI) technology, mixed-signal integrated circuits have become increasingly common. The mixed-design will lead to mutual interference between different circuits in the same ICs, due to parasitic coupling through the silicon substrate. That is the formation of substrate noise and coupling. In digital circuits, different parts of the chip's analog circuit voltage for the substrate are very sensitive, and the numerous high and low speed circuits switching in a large number of parasitic currents in the substrate will produce a transient noise, which was introduced in the analog circuit. Substrate noise will seriously reduce the performance of mixed-signal integrated circuits, along with the chip integration, and it will further increase the operating frequency, which is more significant.

The coupling of the substrate becomes a source of noise, which can lead to errors and system malfunctions, delays in the signal adjustment, low reliability and shortened equipment life [82-85]. These negative effects are even more pronounced in systems with high frequencies.

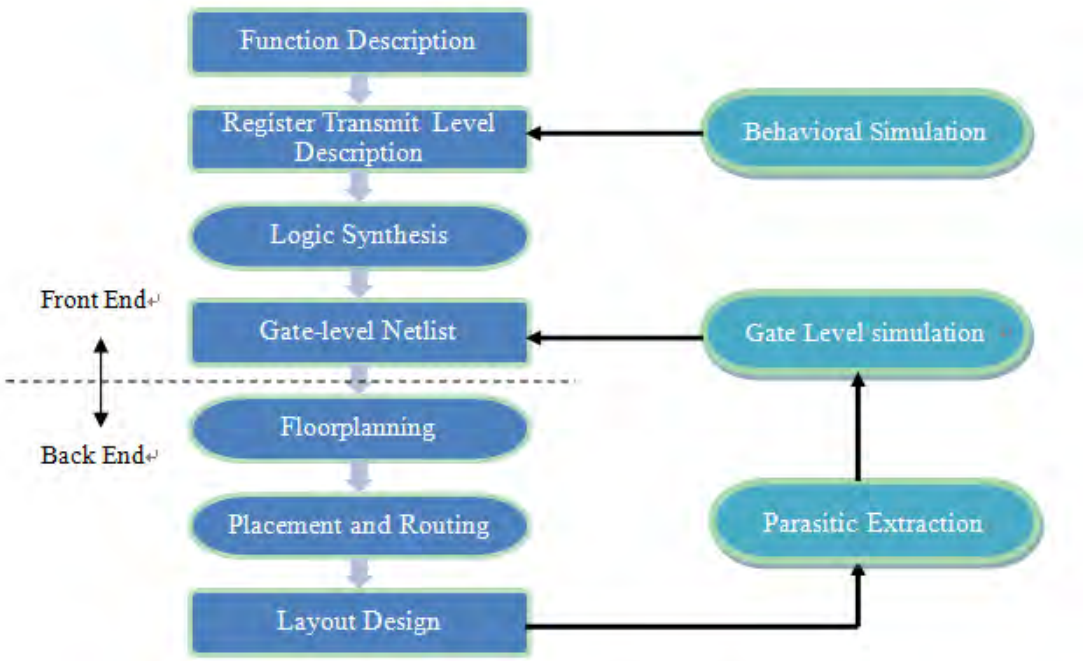


Figure 2-5 A typical IC design flow

A typical IC design flow is shown in Figure 2-5. As can be seen from the chart, there is a step called Parasitic Extraction between the layout design and gate-level circuit simulation. The purpose of this step is to build a model with capacitance, resistance inductance and other components, for electromagnetic coupling that will enable an accurate simulation of the entire circuit. Capacitance receives the majority of the attention, because it critically affects the circuit delay, power consumption and integrity of the signal. Concurrently in the high-frequency circuit, the effects of inductance also become very important, as well as the thermal and mechanical stress phenomena[55, 86]. The eddy current also plays an important role in radio frequency circuits. An integral representation of the eddy-current losses over a conductive substrate has been presented in previous research [87].

The aim of the 3D substrate analysis is thus to efficiently extract the impedance parameters between the contacts and the TSVs which are located on or in the silicon substrate. An efficient impedance extraction tool for contacts and TSVs could help the designer accelerate the design process and optimize the final layout.

Pioneering work in the modeling and analysis of substrate coupling in Integrated Circuits was accomplished by Ranjit Gharpurey [88, 89]. Then Ali M. Niknejad [90], found that Green's Function could be transformed into a numerically stable ??, which would allow it to be used to solve the impedance matrix for 3D conductors placed anywhere in the substrate. This form is appropriate for machine evaluation by finite-precision computations [90].

2.3.1 Green function and Poisson's equation

Posing and solving problems that are described by Poisson Equation is one of the cornerstones of electrostatics. Poisson's Equation is shown below:

$$\Delta V = -\frac{\rho}{\varepsilon} \tag{2.1}$$

where, V is the electrical potential, ρ is the charge density and ε is the dielectric permittivity of the medium[91].

The algorithm is the same in the electrostatic case where Poisson's Equation is replaced by Ohm's law and the diffusion currents are neglected, as shown below

$$\vec{J} = \sigma \cdot \vec{E} \tag{2.2}$$

where, J is the current density in A.m-2, E is the electric field in $V.m^{-1}$ and σ is the conductivity of the medium in $S.m^{-1}$. A different form of Ohm's Law is given by:

$$\Delta\varphi = -\frac{div(\vec{J})}{\sigma} \tag{2.3}$$

where div ($\vec{J}$) is equivalent to $\frac{d\rho}{dt}$, and where ϕ is the potential (V), and Div (J) is not null since an extant current (density) has been imposed.

In Euclidean space, the Laplace operator is usually denoted as ∇^2, so Poisson's Equation is frequently written as shown in 2.4, below.

$$\nabla^2\varphi = -\frac{\rho}{\varepsilon} \tag{2.4}$$

Finding φ for some given ρ and ε is an important practical problem, since this is the usual way to find the electric potential for a given charge distribution.

The above equation may be transformed into an integral equation of the form

$$\phi(r) = \int_V \rho(r')G(r,r')d^3r' \tag{2.5}$$

G is the potential due to a point charge placed at a point r', and G is known as Green's Function[92].

Green's Function can be obtained by solving the following equation:

$$\nabla^2 G = -\frac{\delta(r-r')}{\varepsilon} \tag{2.6}$$

When the source is decomposed into the superposition of many point sources, and if we know the point source field, then by using the superposition principle, we can obtain the same boundary conditions and arbitrary source field. This method for solving equations by mathematical physics is called Green's Function Method.

If Green's Function is known, then equation (2.5) provides a technique for calculating the potential for a point from a known, arbitrarily distributed charge density.

2.3.2 Extraction in 3D Circuits

An efficient algorithm to extract 3D capacitance from multi-layered lossy substrates was presented by Zuochang Ye et al. [93]. This new algorithm uses a Green's Function based solver, and offers a major improvement over the quasi-3D approach. It takes into consideration the sidewalls of the 3D conductors.

To compute the 3D capacitance, the panels of a cuboids's conductor can be grouped into three classes: the horizontal plane, the vertical I, and the vertical II. The positional combinations of each pair of panels can be classified into four types, as shown in Figure 2-6. In Type A, two panels are either bottom or top surfaces of the conductors. In Type B, one panel is horizontal, and the other is vertical. In Types C and D, both panels are vertical. They are parallel to each other in Type C, and perpendicular to each other in Type D.

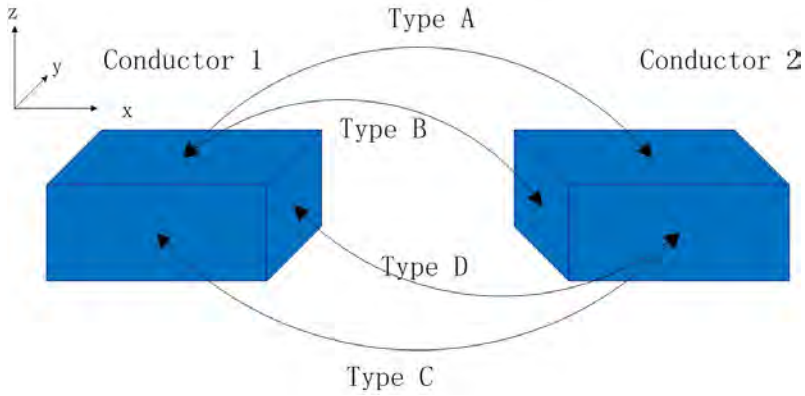


Figure 2-6 Positional relationships of two panels.

In order to obtain the final result, each Type of panel pairss should be discussed separately. More information can be found in [93].

2.4 3D Multi-Level Modeling

Another outcome of forthcoming 2D integration will be the development of a hierarchical modeling concept as well as electrical models of TSVs. A hierarchical model is mandatory in 3D because of the very different granularities that may be considered from the system level down through the TSV level. Using the former models will enable us to follow two paths:

Path A. A Top-Down approach for devising TSV Design Rules

- Matching the estimated thermal power dissipation to the temperature behavior of the TSVs,
- (or) the throughput requirements for the electromagnetic behavior of the TSVs;
- (or) the connection dependant on the TSVs reliability.

Path B. A Bottom-Up approach of assessing the impact of the TSVs on system-level performance.

Derived from geometrical and material data, distributed RLCG electrical models would be proposed and compared to measurements and 3D EM simulations. Similar work would be carried out on the microstrip line and the TSVs, as shown in Figure 2-7.

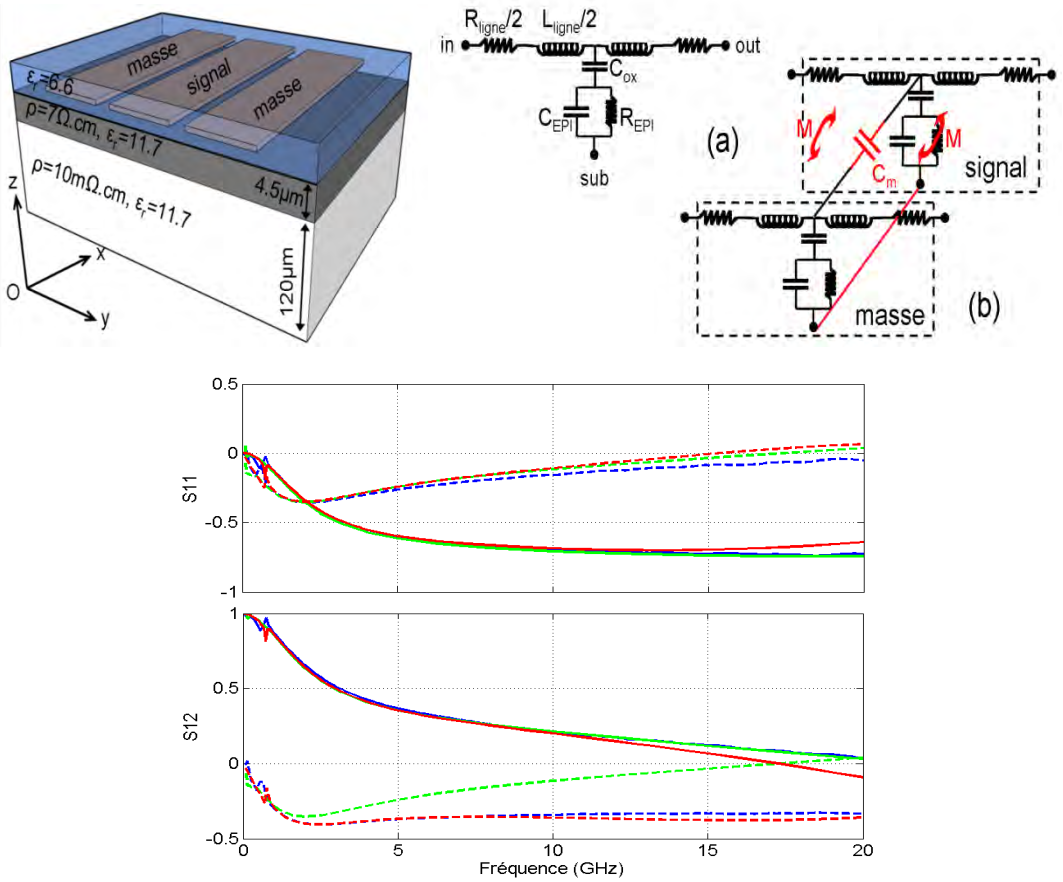


Figure 2-7 Preliminary electrical model for the interconnect in the redistribution layer (coplanar line);

Measurements: Blue is EM simulations, Green is RLCG electrical model, Red is real and imaginary parts of Sij

2.4.1 TSV Electrical Modeling

For RF TSV modeling [94, 95], an ad hoc structure is required to enable RF testing. This structure, called Dual Via Chain, is composed of 2 transmission line segments and 2 TSVs separated by a Back Redistribution Line (BRDL). The Dual Via Chain (Figure 2-8) characterization facilitates obtaining the Scattering Matrix (Sij) of one TSV, after a specific calibration and a de-embedding operation. This measurement is compared to the 3D simulation realized by full wave 3D software. Due to fitting measurements, the material parameters can be adjusted. A spice-like model can then be extracted with frequency dependence for R, L, C and G parameters (Figure 2-8 and Figure 2-9).

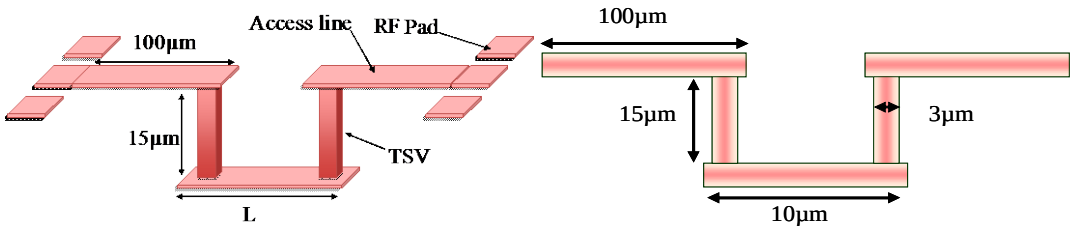


Figure 2-8 Description of the Dual Via Chain for high density TSV

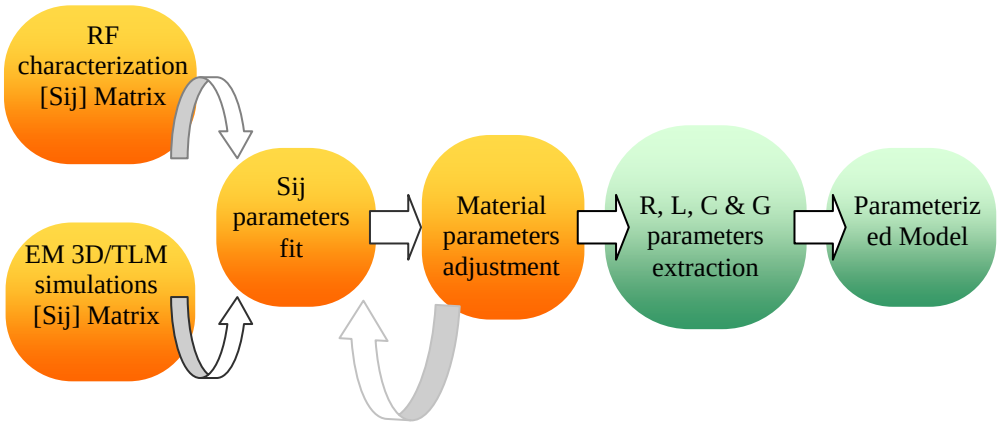
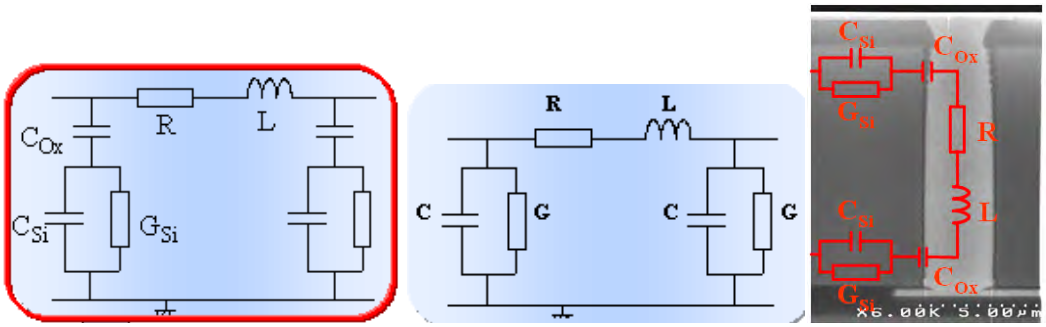


Figure 2-9 Basic methodology for TSV RF modeling

Simulations and characterizations were performed for a 15µm deep and 3µm wide TSV connected by a transmission line of 10µm. An extraction from a π model gave R, L, C and G with a fit between characterization and simulation with a near 5 % rate of error for each parameter (see Figure 2-10 and Figure 2-11). The first model was then enhanced to describe the physical effects, by dividing the total capacitance into 2 parts: oxide capacitance plus silicon capacitance. It is important to note the key role of the silicon conductivity in the TSV behavior, in particular for the R and G parameters, which are representative of the conductive and dielectric losses.



(a) (b) (c)

Figure 2-10 a) π Model of the Dual Via Chain; b) Methodology for TSV RF modeling; c) SEM of the TSV.

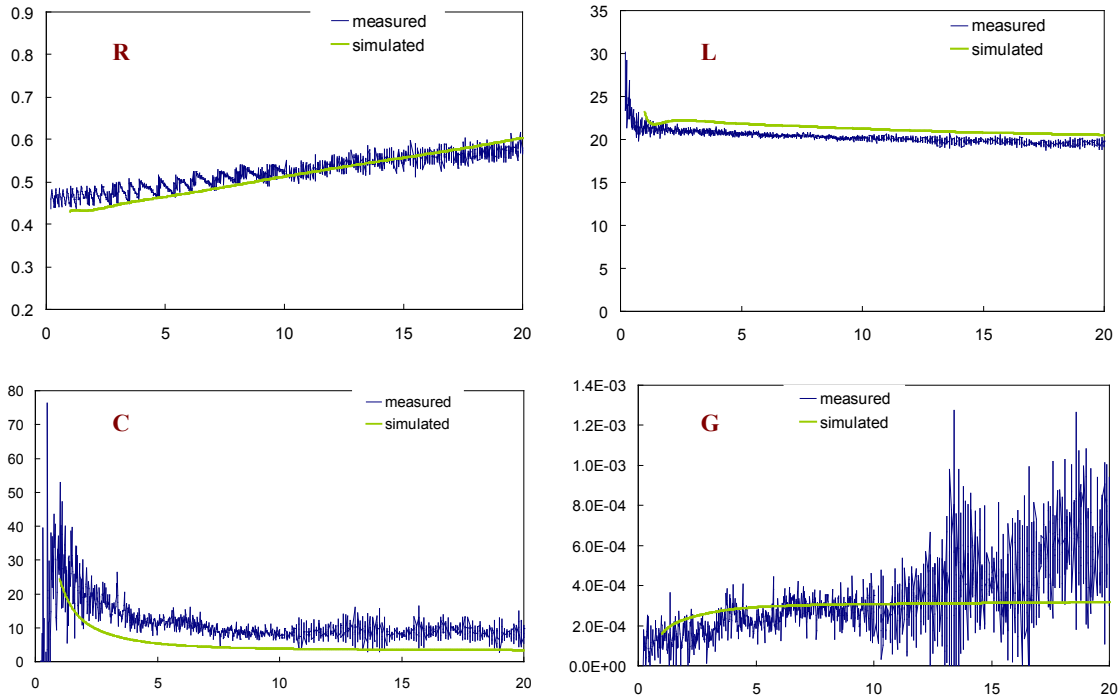


Figure 2-11. R, L, C and G extracted parameters for the (100MHz - 20 GHz) (source: Fraunhofer)

Good agreement between the simulations and measurements validates the appropriatness of the 3D simulation tools for performing a set of varied simulations for TSV performances, predictions and designer recommendations.

The impact of TSV on the delay, rise-time and crosstalk level of propagated signals will be quantified by Time Domain Reflection and Time Domain Transmission (TDR/TDT) simulations for different signal switching conditions. Eye-diagram simulations with the Pseudo Random Bit Sequence (PRBS) will be performed in order to evaluate the limitations of the data rate (Gbps). Noise due to substrate coupling effects will also be analyzed using FEM/Transmission-Line Matrix (TLM)/Impedance Field Method (IFM) solvers. The influence of various factors on the electrical parameters of the interconnects for RFs, such as geometry and material of single generic TSVs and the formation/distance of local interconnect structures, will be computed.

Using the data generated by these simulations, parasitic circuit elements like resistors, capacitors and inductors in transmission line models can be extracted, and later used to derive behavioral models for system level simulations. Furthermore, compact electrical models of the TSV, providing scaling parameters in order to describe various aspect ratio vias, will be developed. These models will also integrate mutual-inductances and capacitive coupling parameters for specific cases.

2.4.2 CAD-EDA

Design rules have to be derived and provided to the designer using simulation results and, when possible, measurement data. These rules will facilitate the thermal management of the structure and minimizing the crosstalk, signal delays, electro-thermal interactions, losses at the RF domain, and so forth. By properly back-annotating the former high-level models with information regarding power, delay, etc., we will be able to obtain meaningful data regarding the 3D implementation of, for instance, a mobile/(HD)TV/ Set Top Box/ Image-sensor application, and match its requirements with the TSV design rules. Parametric simulation studies will also be carried out to derive the rules. Some parameters could be, among others, the geometry, used materials and the material properties.

Currently, Electronic Design Automation (EDA) tools supporting IC packages and modules and SiP designs, are arranged in a manner that assumes and supports all connections between dies going through IC package fabrics, such as: Bumps, wire bonds, traces and vias or Package on Package (PoP) solder balls. With the emerging request for the 3D stacking of dies, this assumption is no longer valid. In order to support 3D architectures, EDA tools will have to be improved to handle direct die-to-die connections within the IC layout tool, including the support of stacked chip configurations, connectivity management, parasitic extraction, analysis and simulation of the stacked ICs.

Methodology, flow and tools will need to be developed to allow flexible stacked IC connectivity between both the different ICs and the final package. Different styles of connectivity will need to be defined and supported to improve cost efficiencies and electrical and thermal results.

The definition and implementation of new methods are needed for flexible floor plan generation, vertical placement and for complex models of interconnects, power grids and clock routings.

TSV-based stacked IC design methodology requires comprehensive development of both the existing flow approach and a totally innovative development of the design flow and associated tools.

Future development must ensure that the following key points are met for the tools and flow:

The stacked IC is correctly modeled to address physical and electrical connectivity.

A set of capabilities are added to the tools to support stacked IC physical connectivity and electrical and thermal modeling.

Development of a design flow for both physical design and electrical analysis,

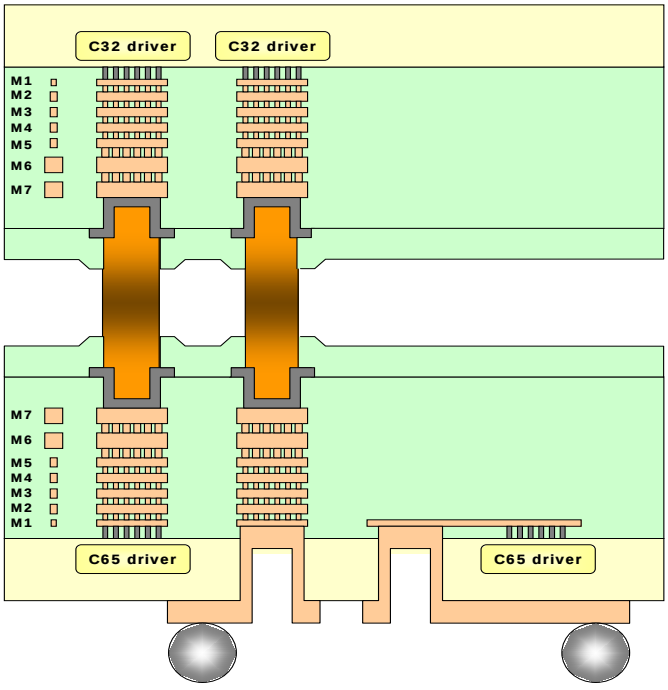


Figure 2-12. Typical SIP approach

In a 3D interconnect approach, for example in 2 dies (as shown in Figure 2-12), the silicon chips will be considered to be one object that must first be analyzed separately. This

meta-object composed of several dies could be then included in a standard SIP analysis (COSIP). The first step would be to utilize a very early floor planning analysis tool that would facilitate defining the main characteristics of the system. We would then focus on obtaining the definition of the DIE stacking structure through a standard format such as. XML

For this group of dies, we will develop CAD flow to achieve the following:

1) Define the TSV, the Bump placement, the automatic alignment, and the update that will be driven from the top to the bottom of the die.

2) Define the power network based on the TSVs and the Bump's direct connection to the power grid.

3) Provide timing analysis of the interconnections through various configurations of the TSV, the stacked dies, and face to face interconnection. This would be based on standard RC parasitic extractions and Static Timing Analysis.

4) A thermal model generation of the system composed of several dies, to utilize later in the package and the PCB simulation.

The TSV design flow development should initially be developed according to the baseline shown below:

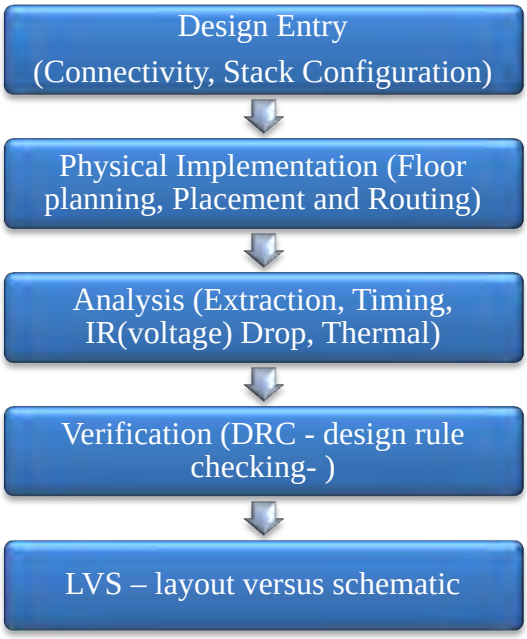


Figure 2-13 TSV Design Flow Approach

The first development target is that of determing how to allow flexible connectivity. This step will define a set of connectivity operations in order to grasp efficient physical design implementations in a hierarchical manner. It will support different implementations of signal nets, power nets and special nets like a clock network.

It will have to depend on specific technological rules such as TSV pitch and TSV size[96] planned for different phases.

Focus must be within the following areas in terms of modeling:

1- TSV layout rules and their affects on stacked IC connectivity.

2- Electrical modeling of TSV and associated components.

3- Thermal modeling of TSV and associated components.

4- Trials of a few configurations and determination of the best implementation connectivity con-figuration (layer stacking, power connectivity, clocking connectivity, feed through to package terminals, etc.).

To create a design flow for a stacked IC implementation, analysis and verification, the method proposed is an extension of current IC design tools and analysis for stacked IC physical implementation and analysis. We will examine some of the following aspects:

1- Information required for supporting stacked IC connectivity.

2- Automatic and interactive physical implementation of stacked IC connectivity.

   a. Signals.

   b. Power and ground.

   c. Special nets.

3- Augment existing physical IC tools to ensure the physical realization of the stacked IC at a different level of flow (IO connectivity, placement routing and layout verification).

4- Modification of IC tools to support the physical implementation.

   a. Placement of the TSV.

   b. Routing of the TSV between different ICs and the package Bumps.

5- Electrical Analysis

How to model the TSV electrical design for interconnect extraction and the use of analysis tools for both implementation and sign-off. Areas to be focused are interconnecting extraction, timing, SI and power integrity, or voltage drop.

Analyze the cross-talk between the vias and between the via and the substrate. One simulation will introduce both capacitive and mutual inductance. The thermo-dynamic behavior of the Via, the interlayer assembly, and the capacity to use the Via for a thermal hole and for possible interferences of RF or high data rate transmissions, will all be analyzed.

6- Thermal Analysis

The development of modeling techniques for thermal analysis will be presented. Thermal analysis can be applied at the stacked level, based on both appropriate reference design, and on actual measurements, so as to improve the methodology of thermal conductivity.

However, modeling all the physical effects will have impacts on the functions of single structures, and on the entire system, such as electromagnetic coupling (EMC), cross talk, interconnect delays, thermal effects and electro-thermal interactions.

Estimation and prediction of interconnects and interfaces at higher description levels, will enable consideration of the timing and the signal integrity during the design process, assuring optimum system performance at the same time.

It is necessary to model for heterogeneous IP for a priori exploration of Function-to-Tier assignments in the 3D context. This work is considered to be a multi-domain and multi-abstraction level optimization problem, since it will be necessary to:

- take into account strong variations in inter-function communication costs using the communication cost model, network topographies and inter-tier technology characteristics using an adequate design kit

- estimate the functional feasibility and performance metrics based on database or performance modeling

- globally minimize the power, equalize the areas of all tiers, maximize the robustness of the parametric dispersion and minimize temperature variations or sensitivity of specific functions to temperature variation.

The main difficulty with a priori exploration is that the choice of architectural block parameters must be made according to non-ideal effects (implementation technology, sensitivity to noise and temperature variations, and dispersion) which are not known. It is therefore essential to determine the application-defined design space and to map this to a technology-defined design space, for each architectural variant that is to be considered. The development of this approach will thus rely heavily on high-level models, as well as on the exploitation of design databases for data mining techniques and for the investigation of the suitability of Pareto fronts in order to optimize the search speed and database size, and for estimation methods. The combination of bottom-up performance space models as a way to improve the overall efficiency of the flow will be investigated.

It is also important to investigate a design flow to analyze the performance of hard and soft real-time applications on a predictable and compostable 3D MPSoC (Multiprocessor System-on-Chips) platform. Furthermore, performance and cost tradeoffs can be enabled, such as application qualities like picture quality and reliability, versus energy costs. As a further development, it may be possible to guide the system designer through the design space, or to synthesize part of the system architecture, based on the inputs of the architect. The design flow will take processor, interconnect, and memory performance into account when computing the area, the energy costs and the performance. At completion the built-in tests will include recovered loops, to avoid fault divergence behavior.

The mapping problem is believed to be feasible for this class, as streaming (as compared to Digital Signal Processing) applications are inherently parallel, and their memory access can be distributed over parallel processors. Re-configurable subsystems that have been designed often contain coarse-grained reconfigurable processors. Compilers for coarse-grained reconfigurable architectures are a key challenge. In order to be efficient in terms of performance and energy, coarse-grained reconfigurable architectures shift complexity from the hardware to the compiler. The intrinsic hardware efficiency is only obtained if the compiler exploits the specific hardware features of the target architecture. Making a compiler for a coarse-grained reconfigurable architecture is known to be an NP-Hard (Clay) problem. Therefore, novel heuristic methods are needed for transformations, clustering, scheduling, and resource allocation. The choices made during one of these compiling phases, influence the performance that can be achieved in other phases. Therefore, such heuristics should interwork, in order to find a global, nearly optimal solution. These tools include compilers, simulators and software debuggers, and are needed for programming the reconfigurable subsystem. The tools are used to implement a realistic application on the reconfigurable subsystem, which is necessary for its evaluation for the 3D integration technology, in terms of performance, energy-consumption, and reliability.

Very often demonstrators are dedicated to Wireless applications driven by footprint optimization, such as digital part stacked on an analog and RF device [97]. .

A predilection demonstrator can be our general project, of some typoe of detector for research experiments or for an imaging device in Medical or Spatial applications (see Figure 2-14).

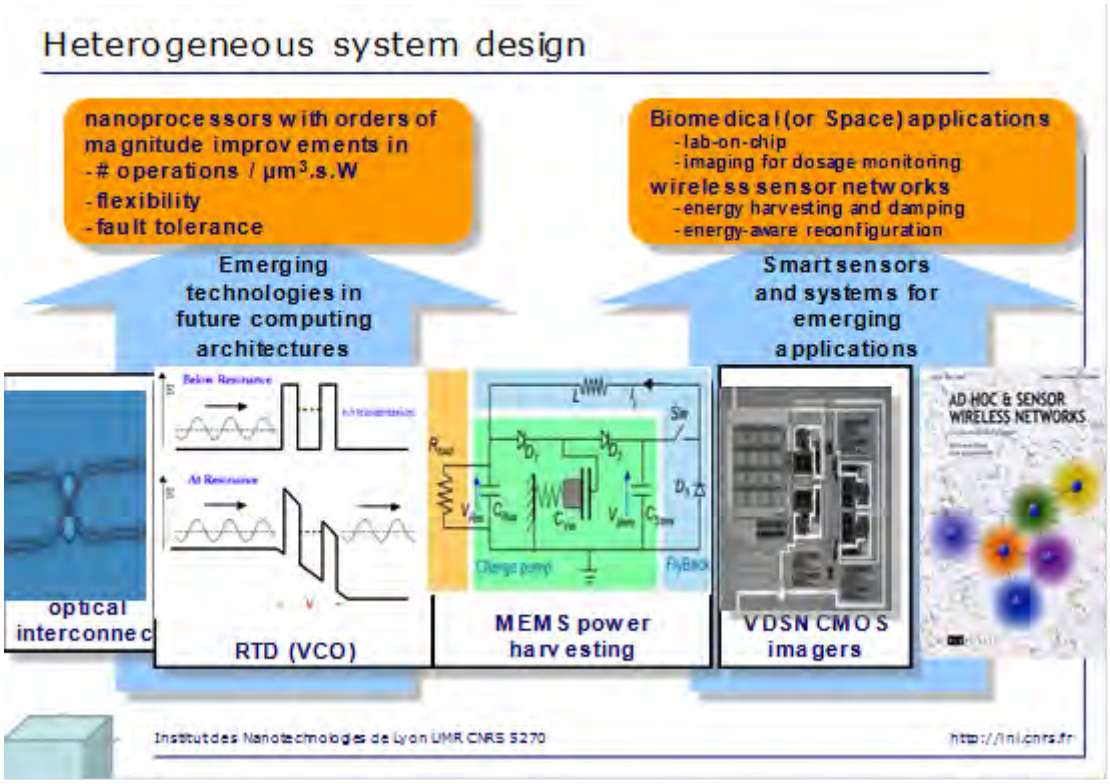


Figure 2-14 Heterogeneous System Design.

The purpose here is to develop an advanced technology in order to have the front-end or local intelligence ASIC closely embedded on the instrument. This would eliminate as much wire or Bump bonding as possible, and would improve performance at the same time (for example by creating less noise and material) and would result in more compact devices.

The direct interconnect is another novel feature that will be addressed in future projects, first with flip-chips and then with 3D vertical interconnect based technology, like the TSV. This would require numerous interfaces, including digital and analog processing. The current design has those blocks connected traditionally by several metal layers. However, to increase design flexibility and reduce costs, this design could be split into several (ideally two) chips. One chip would be dedicated to the analog process (for 65 nm processing or less), and the other chip would be dedicated to the high density digital process (for 32 nm or less). For this splitting process, it is necessary to modify the design of the different blocks in consideration of the electrical effects of the new physical interconnect, based on the TSV connections. The designers would use the different tools and the interconnect model to regenerate a new netlist where the TSV connections would appear as specific components. Blocks partitioned into chips would have to handle the high frequency links and low voltage drop connections.

All the simulations would have to be performed to verify the splitting of the original design into n chips, and to ensure that the TSV connections would not disturb the electrical performances of the n chips. These simulations would use pre-studied electrical and thermal models. The results would be compared to previous results, before splitting. This would involve mixed digital or analog simulations and would have to handle high frequency line effects related to the TSV modeling. When needed, line adaptation would be added to compensate for any spurious effects caused by the TSV connection.

A test plan would be adapted to the new device interconnect, as well as a reference board to validate the chip.

3D multi-processor computing architecture design can also be used for FPGA (Field Pogrammable Gte Aray) (prototype platform) and silicon implementation [98]. The size of the reconfigurable sub-system that could be demonstrated might be limited by the size of the FPGA. The application may not meet real-time constraints on the FPGA demonstrator.

A technological solution would be developed for the vertical stacking of dies, and for a reusable system architecture that encompasses modeling, system design integration, design automation and physical demonstrators (3D-ICs) using TSV technology and experience for the 3D integration of the dies. The last but not the least important point is that market leaders in EDA systems would have to bring forth their know-how in design flows and CAD tools[99].

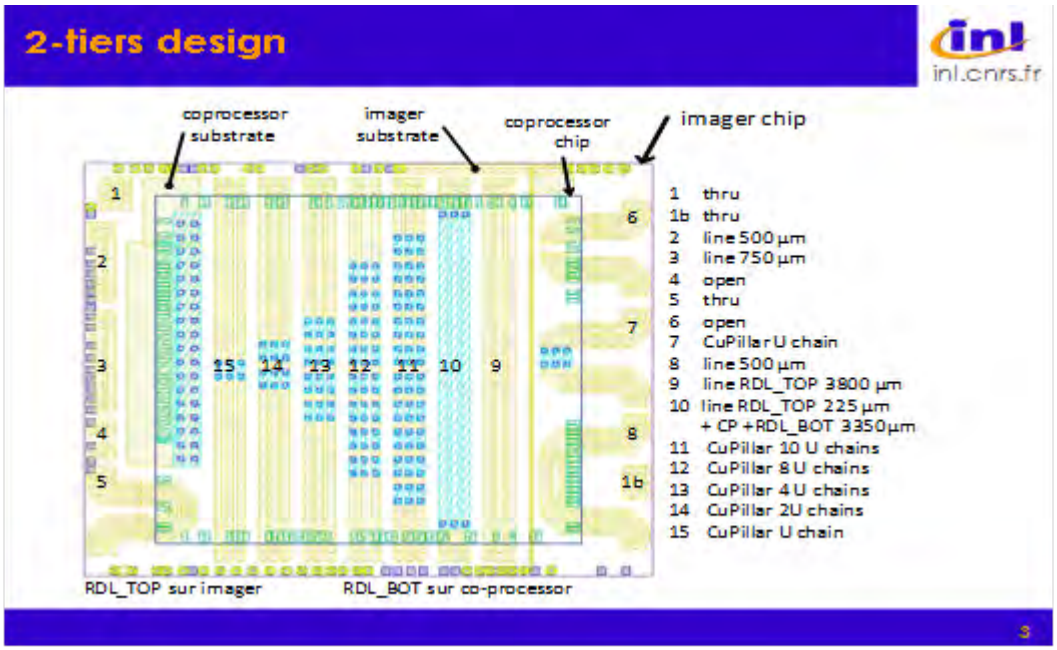


Figure 2-15 Advanced interconnect technology and packaging objectives (LETI)

Defining a hierarchical modeling concept as shown in Figure 2-16 is quite a complex task because of the following identified requirements:

- The concept must be multi-scale as it must model the entire 3D circuit from the system level down to the TSV level;
- It must be flexible enough for some designers to perform simulations tier by tier, and others to simulate a given function that is split over multiple tiers;
- In terms of geometrical information and material information, using TSV modeling results, we would thus be able to use two separate types of models: *fixed extracted from measurement results* and *scalable/predictive* models (extracted from electromagnetic simulation with calibration to measurements).

- It must account for diverse effects such as: crosstalk between TSV and thermal dissipation issues, analog: noise, coupling, thermal and bandwidth,digital/RTL (VHDL or System C), delay and logic levels …

Due to different requirements at any given point in the design flow for 3D systems (system, analog or digital), multiple representations of objects may be required, such as ELDO/SPICE, Verilog-AMS or Liberty Timing Library. Flexibility would be needed to explore changes in the technology, data width and TSV parameters such as the density of the TSVs, where density relates to the aspect ratio and to what connection density could be achieved, which is a very key point. This requires unified interfaces between the models, parameterized in terms of the geometrical information and the material information.

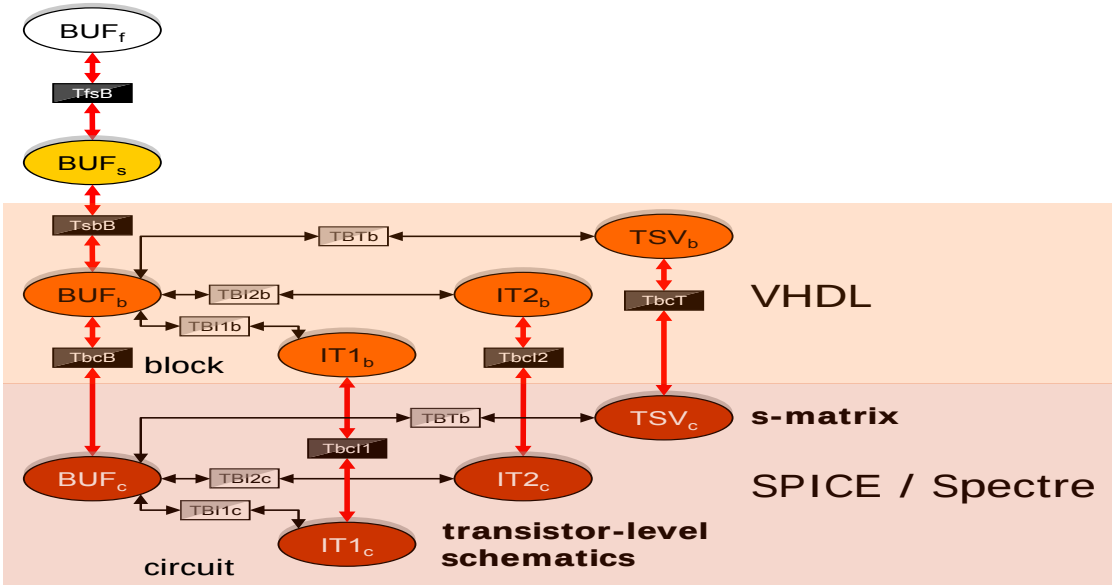


Figure 2-16 Definition of model abstraction for 3D integration – Hierarchical Modeling Concept

3 3D Substrate Impedance Extraction (3D-IE)

Owing to the inefficiency of numerical methods for substrate model, effective tools are needed to accelerate the device and circuit design, without significant loss of accuracy and reliability. The tool should be used to analyze the practical layout, to grasp the electric performance of the circuit and to calculate the substrate impedance matrix to analyze the substrate coupling. On this topic, some research programs have been published in recent years under electrical [37]-[41], thermal [100], or stress [101]-[54] analysis. A BEM-based substrate extraction has been proposed [38] but it's only applied to analyze coupling between contacts laid on the top surface of substrate but not 3D TSV structure. Parasitic coupling capacitance is analyzed in various configurations in [9] depending on TSV is surrounded by top, bottom or side nearby interconnect wires. However, the TSV model is simplified by neglecting the TSV inductance, the capacitance of the oxide and by making the assumption of a high-resistivity substrate. So, we propose a new based on transmission-line matrix (TLM)[102, 103] method to extract the impedance between contacts and TSVs which is applicative for multi-layer substrate.

In this chapter, this new method relying on TLM over multi-layered substrate or Green Kernels is introduced. It can model these effects, in the bulk. The algorithm details will be given to calculate the Z parameters between on top or embedded contacts and TSVs of a multi-layers substrate. Then this modeling approach is validated in the third part by performing frequency-domain analysis through Z-parameters[104]. At last, the conclusion summarizing the essential points and reports on-going works will be declared.

3.1 3D-IE Introductions

As described above, high density integration and high frequency system make substrate noise coupling become one of the most significant considerations in the design due to its significant impact on the performance of ICs. The main aim of the 3D substrate analysis is to efficiently extract the Z impedance parameters between the contacts and TSVs which are located on or into the silicon substrate. An efficient impedance extract tool for contacts and TSVs could help the designer to accelerate the design and optimize the final layout. According to Ted Vucurevich, among all EDA challenges for 3D SIC designs, tools and methodologies for 3D IC testing are regarded as the "No.1 challenge".[105]

As in planar technologies, 3D interconnects can be built as an 'RLCG' equivalent electrical model on a Π or a T network. Often, a simple compact model has been constructed by modeling the substrate as a simple node (Figure 3-1(a)). However, this assumption is only

viable when the substrate is highly conductive, in low and medium frequency domains, and is not suitable for the multi-layer substrates. In high frequencies, the couplings of the substrate become a source of noise, which can lead to errors and malfunctions of systems, delays in adjusting the signal, low reliability and short life of equipment; consequently substrate effects must be taken into account by modeling on it as a 'RLCG' network for instance Figure 3-1(b). That is the reason why a substrate extraction method is needed.

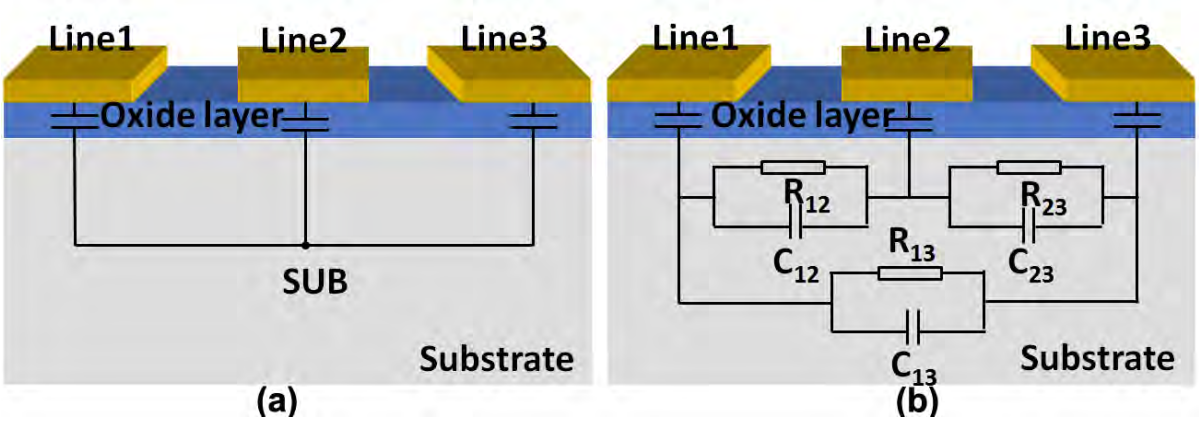


Figure 3-1 Representation of the substrate network compact model and the oxide layer capacitances (a) Coplanar waveguide atop a conductive substrate without epitaxial layer. (b) Coplanar waveguide atop a high resistive substrate without epitaxial layer.

3.1.1 Substrate analysis

Generally, the Z parameters could be defined as

$$Z_{mn} = \frac{V_m}{I_n}\bigg|_{I_{k\neq n}=0} \tag{3.1}$$

In practical operation, by injecting a unit current excitation at n-th point and calculate the resulting voltage at m-th point, we can get the impedance Zmn between contact m and contact n directly.

If we can get the resulting potential distribution of the substrate caused by the unit current, we could get the Z parameters by equation (3.1) directly.

Under quasi-static conditions, the potential over the substrate satisfies Laplace's equation

$$\nabla^2\varphi(x,y,z) = 0 \tag{3.2}$$

It can also be written as

$$\left(\frac{\partial^2}{\partial x^2}+\frac{\partial^2}{\partial y^2}+\frac{\partial^2}{\partial z^2}\right)\varphi(x,y,z) = 0 \tag{3.3}$$

After a bi-dimensional spatial fast Fourier transform (FFT)[106] in x, y direction, we transform the spatial domain coordinates to spatial-frequency domain[107] which is used widely in digital image processing.

So, the above equation is transformed to be

$$\frac{\partial^2 \Phi}{\partial z^2} - k_x{}^2 \Phi - k_y{}^2 \Phi = 0 \tag{3.4}$$

where Φ is the potential in spatial-frequency domain and k_x, k_y are the spatial-frequency variables in two orthogonal directions.

From the definition of current density $j_Z = \sigma^* E_Z$ (σ^* is the complex conductivity) and $E_Z = -\frac{\partial \varphi}{\partial z}$ we can get

$$j_z = -\sigma^* \frac{\partial \varphi}{\partial z} \tag{3.5}$$

In the spatial-frequency domain, it changes to

$$J_z\left(k_x, k_y, z\right) = -\left(\sigma + j\omega\varepsilon\right)\frac{\partial \Phi\left(k_x, k_y, z\right)}{\partial z} \tag{3.6}$$

After derivation calculus of the above equation,

$$\frac{\partial J_z}{\partial z} = -\left(\sigma + j\omega\varepsilon\right)\frac{\partial^2 \Phi}{\partial z^2} \tag{3.7}$$

From equations(3.4) and (3.7) we have

$$\frac{\partial J_z}{\partial z} = -\left(\sigma + j\omega\varepsilon\right)\left(k_x{}^2 + k_y{}^2\right)\Phi \tag{3.8}$$

Rewrite equations(3.6) and(3.8), finally one can get

$$\begin{cases} \dfrac{\partial \Phi}{\partial z} = -\dfrac{J_z}{\left(\sigma + j\omega\varepsilon\right)} \\ \dfrac{\partial J_z}{\partial z} = -\left(\sigma + j\omega\varepsilon\right)\left(k_x{}^2 + k_y{}^2\right)\Phi \end{cases} \tag{3.9}$$

These equations indicate the relationship between z direction current density and the potential distribution in the spatial-frequency domain. In the following part, we will find equation(3.9) is formally identical to the so-called telegraphers' equations.

3.1.2 Transmission line method; brief recalls

In general form, a Transmission Line (TL) is a pair of conductors linking together two electrical systems (source and load, for instance), with a forward and return paths; for cases where the return path (and the forward) is floating, a third conductor (or more) is introduced as the grounding shield. For microwaves, they are waveguides[108]. In our case, the propagation of EM waves, their interferences, through the silicon substrate, is among the most serious obstacles in the steady trend towards integration of present day microelectronics. In fact the TL modeling method (TLM)[102] is well established; it can be seen as a more physical interpretation of the mathematical developments. Transmission lines could be described by the distributed parameters. The basic equations are the same with the 1D case. For uniform transmission line, an infinitesimally short segment of the transmission line could be treated as lumped parameters. It has resistance R0dz, inductance L0dz, capacitance C0dz and leakage conductance G0dz. The equivalent model of the infinitesimally tiny segment of the uniform transmission line is shown in Figure 3-2(b). Figure 3-2(d) gives the equivalent

model for the entire transmission line which is the cascade connection of the infinitesimally short segment model.

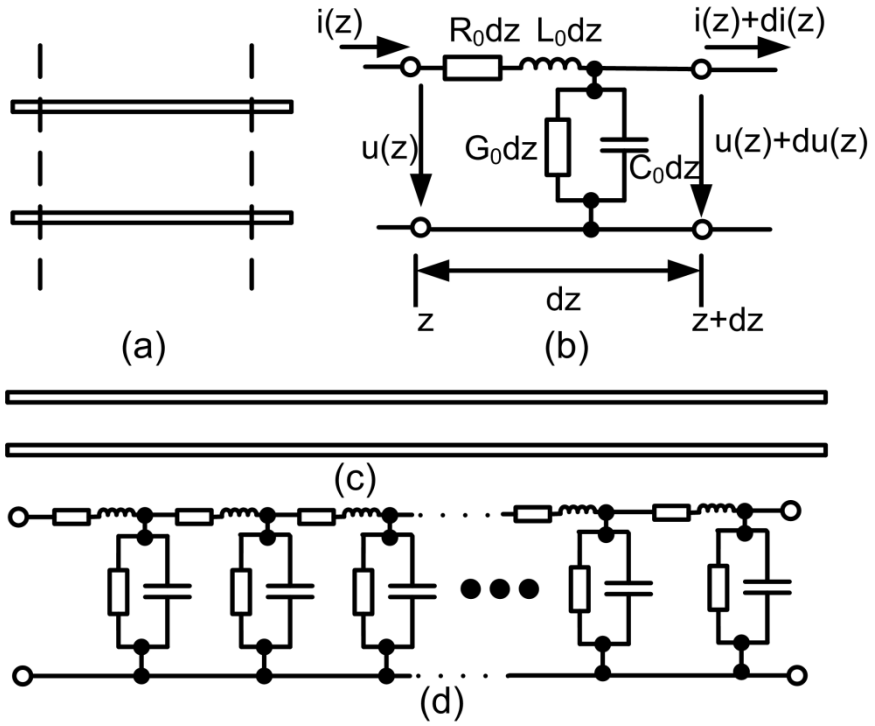


Figure 3-2 (a) Infinitesimally short segment of the transmission line. (b) Equivalent model of the short segment. (c) Whole transmission line. (d) Whole transmission line RLCG model which is a cascade connection of the infinitesimally short segment model.

In Figure 3-2(b), from Kirchhoff's law,

$$\begin{cases} du(z,t) = -R_0 \cdot dz \cdot i(z,t) - L_0 \cdot dz \cdot \dfrac{\partial i(z,t)}{\partial t} \\ di(z,t) = -G_0 \cdot dz \cdot u(z,t) - C_0 \cdot dz \cdot \dfrac{\partial u(z,t)}{\partial t} \end{cases} \tag{3.10}$$

Equation (3.10) also could be written as

$$\begin{cases} \dfrac{\partial u(z,t)}{\partial z} = -R_0 \cdot i(z,t) - L_0 \cdot \dfrac{\partial i(z,t)}{\partial t} \\ \dfrac{\partial i(z,t)}{\partial z} = -G_0 \cdot u(z,t) - C_0 \cdot \dfrac{\partial u(z,t)}{\partial t} \end{cases} \tag{3.11}$$

The equation (3.11) is call as the Telegrapher's Equations.

In the case of the harmonic wave, the voltage u(z,t) and current i(z,t) could be represented as

$$\begin{aligned} u(z,t) &= \mathrm{Re}\left\{U(z)e^{j\omega t}\right\} \\ i(z,t) &= \mathrm{Re}\left\{I(z)e^{j\omega t}\right\} \end{aligned} \tag{3.12}$$

Invoke (3.12) into (3.11), one can get

$$\begin{cases} \dfrac{dU(z)}{dz} = -\left(R_0 + j\omega L_0\right)\cdot I(z) = -Z_1 I(z) \\ \dfrac{dI(z)}{dz} = -\left(G_0 + j\omega C_0\right)\cdot U(z) = -Y_1 U(z) \end{cases} \tag{3.13}$$

where $\begin{cases} Z_1 = R_0 + j\omega L_0 \\ Y_1 = G_0 + j\omega C_0 \end{cases}$ and they are the impedance per unit and admittance per unit, respectively.

3.2 Algorithm Analysis

In this part, we introduce the algorithm of 3D-IE methods. The impedance extraction algorithm will be given for the single layer top surface model, multi-layer top surface model, contacts embedded in the substrate and impedance between contacts and TSVs respectively.

Rewrite equation (3.9) and equation (3.13) here,

$$\begin{cases} \dfrac{\partial \Phi}{\partial z} = -\dfrac{J_z}{\left(\sigma + j\omega\varepsilon\right)} \\ \dfrac{\partial J_z}{\partial z} = -\left(\sigma + j\omega\varepsilon\right)\left(k_x{}^2 + k_y{}^2\right)\Phi \end{cases}$$

$$\begin{cases} \dfrac{dU(z)}{dz} = -Z_1 I(z) \\ \dfrac{dI(z)}{dz} = -Y_1 U(z) \end{cases}$$

Compare equation (3.9) and equation (3.13), we will find that they are formally identical to each other.

Line voltage U in TLM corresponds to the transformed potential distribution Φ and the line current I corresponds to z component of the current density in the transformed domain J_z. That means the substrate analysis problem can be related to an equivalent transmission line problem.

Take the derivative of equation(3.13) with respect to z,

$$\begin{cases} \dfrac{d^2U(z)}{dz^2} - Z_1 Y_1 U(z) = 0 \\ \dfrac{d^2I(z)}{dz^2} - Z_1 Y_1 I(z) = 0 \end{cases} \tag{3.14}$$

Define propagation constant as

$$\gamma = \sqrt{Z_1 Y_1} = \sqrt{\left(R_0 + j\omega L_0\right)\left(G_0 + j\omega C_0\right)} \tag{3.15}$$

and characteristic impedance as

$$Z_0 = \sqrt{\frac{Z_1}{Y_1}} = \sqrt{\frac{\left(R_0 + j\omega L_0\right)}{\left(G_0 + j\omega C_0\right)}} \tag{3.16}$$

Then equation (3.14) changes to

$$\begin{cases} \dfrac{d^2U(z)}{dz^2} - \gamma^2 U(z) = 0 \\ \dfrac{d^2I(z)}{dz^2} - \gamma^2 I(z) = 0 \end{cases} \tag{3.17}$$

Its general solution is

$$\begin{cases} U(z) = A_1 e^{-\gamma z} + A_2 e^{\gamma z} \\ I(z) = B_1 e^{-\gamma z} + B_2 e^{\gamma z} \end{cases} \tag{3.18}$$

where A1,A2,B1 and B2 can be fixed by the boundary condition.

Via equation(3.13), the relationship between A_1, A_2, B_1 and B_2 can be gotten. From equation (3.13)

$$I(z) = -\frac{1}{Z_1}\frac{dU(z)}{dz} = \frac{1}{Z_0}(A_1 e^{-\gamma z} - A_2 e^{\gamma z}) \tag{3.19}$$

So $B_1=A_1/Z_0$ and $B_2=-A_2/Z_0$, and equation (3.18) rewrite as

$$\begin{cases} U(z) = A_1 e^{-\gamma z} + A_2 e^{\gamma z} \\ I(z) = \dfrac{1}{Z_0}(A_1 e^{-\gamma z} - A_2 e^{\gamma z}) \end{cases} \tag{3.20}$$

So if we fix the A1 and A2 in these equations, we can get the expression of U and I.

From equation (3.9) and equation (3.13), the equivalent transmission lines have corresponding specific propagation constant γ and characteristic impedance Z_0 which are

$$\begin{cases} \gamma = \sqrt{\left(k_x^{\,2} + k_y^{\,2}\right)} \\ Z_0 = \dfrac{1}{(\sigma + j\omega\varepsilon)} \cdot \dfrac{1}{\gamma} \end{cases} \tag{3.21}$$

Due to the relationship between U and I in transmission line, it is easy to know, the relationship between Φ and J_z can be gotten in the same way.

3.2.1 Single layer top surface model

The relationship between the substrate model and its equivalent transmission line is depicted in Figure 3-2 (Notice the direction current of I_2', it flows out of the port, so note it as I_2' to distinguish it from injecting in current I_2).

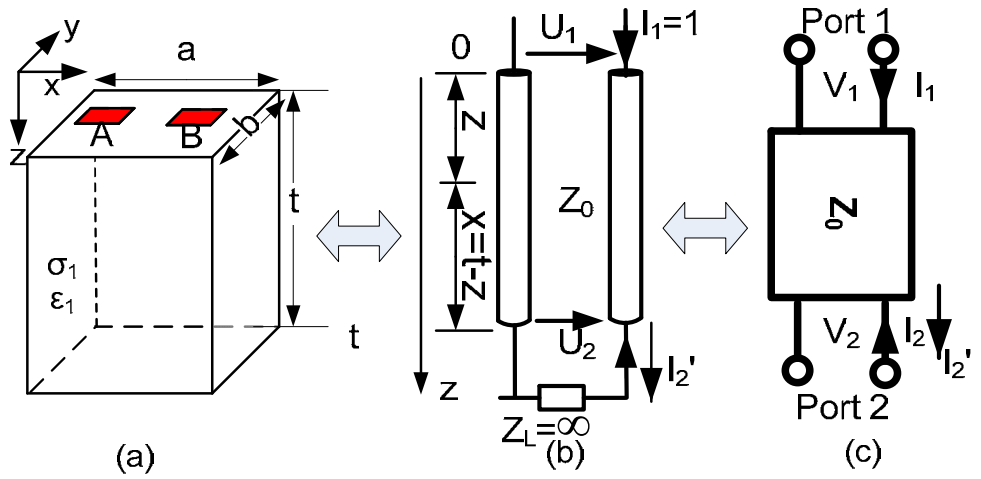


Figure 3-3 (a) presents two contacts laid on top surface of a single layer substrate. (b) Its equivalent TLM Transmission line model. (c) Equivalent two-port network model. Because the current that flow out the bottom surface of (a) is zero, so the load impedance (Z_L) in (b) is positive infinity.

In the above example, the characteristic impedance of the transmission line model in Figure 3-2 (b) ought to be calculated through equation (3.21) from the substrate property (σ1, ε1 and t) in Figure 3-2 (a).

In substrate analysis problem (Figure 3-2 (a)), we can get the impedance Z_{AB} between contacts A and B by injecting a unit current excitation at one contact and calculate the resulting voltage at the other one. Similarly, we could get all the Z parameters via equation(3.1) directly.

According to equation(3.9) and equation(3.13), in the equivalent model Figure 3-2 (b), we need to know the U_1 resulted by a unit injection current I_1.

In Figure 3-2 (a), the boundary condition of the bottom surface is

$$\frac{\partial \vec{E}}{\partial z} = 0 \tag{3.22}$$

From $J = \sigma^* E$ we get

$$J_z = \frac{\partial J}{\partial z} = 0 \tag{3.23}$$

Accordingly, that means the output current I_2' in Figure 3-2 (b) satisfy

$$I_2' = 0 \tag{3.24}$$

So by now, the problem changes to calculate the input voltage U_1 under the condition of the unit input current and open load.

The equivalent model is as in Figure 3-2 (b).

In order to get the coefficient A_1 and A_2 in equation(3.20), assume the output voltage U_2 and output current I_2' in Figure 3-2 (b) are given. Invoke $U(z=t)=U_2$ and $I(z=t)=I_2'$ in equation(3.20) ,

$$\begin{cases} U_2 = A_1 e^{-\gamma t} + A_2 e^{\gamma t} \\ I_2' = \frac{1}{Z_0}(A_1 e^{-\gamma t} - A_2 e^{\gamma t}) \end{cases} \tag{3.25}$$

So,

$$\begin{cases} A_1 = \frac{1}{2}(U_2 + Z_0 I_2')e^{\gamma t} \\ A_2 = \frac{1}{2}(U_2 - Z_0 I_2')e^{-\gamma t} \end{cases} \tag{3.26}$$

Invoke A_1 A_2 back to the equation(3.20),

$$\begin{cases} U(z) = \frac{1}{2}(U_2 + Z_0 I_2')e^{\gamma(t-z)} + \frac{1}{2}(U_2 - Z_0 I_2')e^{-\gamma(t-z)} \\ I(z) = \frac{1}{2}\left(\frac{1}{Z_0}U_2 + I_2'\right)e^{\gamma(t-z)} - \frac{1}{2}\left(\frac{1}{Z_0}U_2 - I_2'\right)e^{-\gamma(t-z)} \end{cases} \tag{3.27}$$

From the definition of hyperbolic function, equation(3.27) could be written as

$$\begin{cases} U(z) = U_2 \cosh(\gamma(t-z)) + Z_0 I_2' \sinh(\gamma(t-z)) \\ I(z) = \frac{U_2}{Z_0} U_2 \sinh(\gamma(t-z)) + I_2' \cosh(\gamma(t-z)) \end{cases} \tag{3.28}$$

and note x=t-z as in Figure 3-2 (b),

$$\begin{cases} U(x) = U_2 \cosh(\gamma x) + Z_0 I_2' \sinh(\gamma x) \\ I(x) = \frac{U_2}{Z_0} U_2 \sinh(\gamma x) + I_2' \cosh(\gamma x) \end{cases} \tag{3.29}$$

In Figure 3-2 (b), $U_1 = U(z=0) = U(x=t)$ and $I_1 = I(z=0) = I(x=t)$. So the input voltage U_1 and input current I_1 in matrix forms are

$$\begin{bmatrix} U_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \cosh(\gamma t) & Z_0 \sinh(\gamma t) \\ \frac{1}{Z_0}\sinh(\gamma t) & \cosh(\gamma t) \end{bmatrix} \begin{bmatrix} U_2 \\ I_2' \end{bmatrix} \tag{3.30}$$

where t is the thickness of the substrate layer, Z_0 and γ is calculated by(12).

So from equation(3.24) and equation(3.29), the value of the U_1, U_2 can be calculated directly. We define the input impedance in spatial-frequency domain as Z_{in}, so it should satisfy,

$$Z_{in} = Z_{11} = \frac{U_1}{I_1} = Z_0 \cdot \coth(\gamma t) \tag{3.31}$$

Accordingly, on the top surface it should also satisfy

$$\Phi(k_x, k_y, z=0) = Z11(k_x, k_y, z=0) \cdot J_z(k_x, k_y, z=0) \tag{3.32}$$

So, to summarize so far, the general process is, firstly, to calculate the Zin by equation(3.29) and equation(3.31), then, get the potential distribution by inverse transformation of equation(3.32) (i.e. the voltage), and at last, to get the Z parameter by equation(3.1).

3.2.2 Multi-layers top surface model

The only difference between single layer top surface substrate impedance extraction and the multi-layer one is the calculation of Z_{in} (cf. equation(3.31)).

For the single layer equivalent transmission line model (Figure 3-3), each layer could be equivalently model as a two-port network as Figure 3-3(c).

There are a number of alternative sets of parameters that can be used to describe a linear two-port network; the usual sets are respectively called Z, Y, H, G and ABCD parameters.[109, 110] The conversation between them can be found in Annex. Here we will use the Z and ABCD parameters.

The ABCD-parameters are known variously as chain, cascade, or transmission line parameters. It's very suitable to present the cascade connection model.

Based on the definition of ABCD parameters, for two-port networks as shown in Figure 3-3(c),

As note $I_2' = -I_2$, it should be

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2' \end{bmatrix} \tag{3.33}$$

Compare equation(3.30) and equation(3.33),

$$\begin{aligned} A &= \cosh(\gamma t) \qquad B = Z_0 \sinh(\gamma t) \\ C &= \frac{1}{Z_0}\sinh(\gamma t) \quad D = \cosh(\gamma t) \end{aligned} \tag{3.34}$$

So based on a single layer substrate could be equivalently modeled as a two-port network, a multi-layers system as in Figure 3-4(a) could be modeled as the cascade connection of two-port networks (Figure 3-4 (b)).

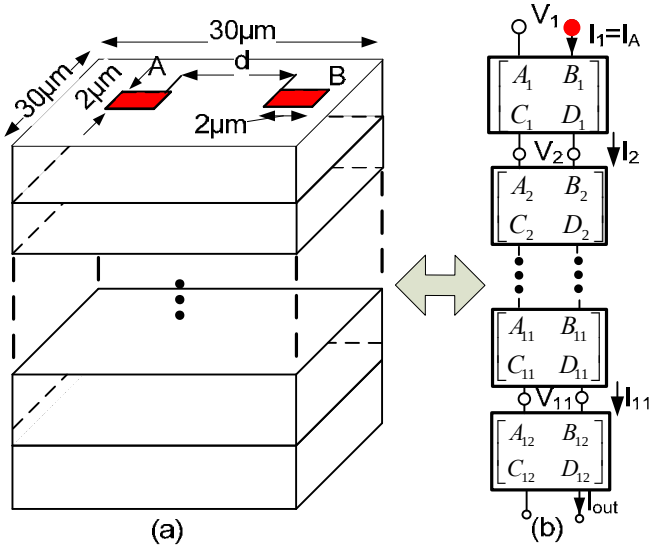


Figure 3-4 Multi-layers top surface contacts geometry structure to be tested (a) and its corresponding TLM model (b). The dimension of the substrate is 30µm, 30µm in X, Y. Two square contacts of 2µm×2µm are located on the top surface of this multi-layer substrate with a separation distance d.

As shown in Figure 3-4, what we need to know is the voltage on contact B (i.e. V_1 in the right model). The I_{out} and I_1 is given from the boundary condition (i.e. I_1=1 and I_{out}=0).

The total ABCD-parameter between port-top and port-bottom (Figure 3-4(b)) could be calculated by matrix multiplication of each single layer as follows.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \mathrm{a}_1\mathrm{a}_2\cdots\mathrm{a}_n = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix}\begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix}\cdots\begin{bmatrix} A_n & B_n \\ C_n & D_n \end{bmatrix} \tag{3.35}$$

Once getting the total ABCD-parameter between port-top and port-bottom by equation(3.35), the multi-layer substrate can be treated as a single layer model as in Figure 3-3.

The Z parameters can be converted from ABCD-parameter by equation(3.36).

$$Z = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} = \begin{bmatrix} \frac{\mathrm{A}}{\mathrm{C}} & \frac{\det(ABCD)}{\mathrm{C}} \\ \frac{1}{\mathrm{C}} & \frac{\mathrm{D}}{\mathrm{C}} \end{bmatrix} \tag{3.36}$$

Then Z_{11} used as Z_{in} in equation(3.31) can be gotten from equation(3.36). The following impedance extraction steps for multi-layered substrate will be exactly same as the single layer top surface contact model in section 3.2.1.

Define Z_0 the characteristics impedance (Electric and magnetic fields modulus ratio); Z_L the charge impedance, L the distance from the load, we can extract an input impedance, said Zl (=V1/I1), function of the load impedance Zl+1 (l: layer number) as:

$$Z_l = Z_0 \frac{Z_{l+1} + Z_0 \tanh \gamma L}{Z_0 + Z_{l+1} \tanh \gamma L} \tag{3.37}$$

It is straight forward to program this iterative solution (versus substrate depth, or layers).

3.2.3 Contacts embedded in multi-layers substrate

The principal strength of the 3D-IE is it is well dedicated to embedded contacts. Two different cases as partial contacts embedded and all contacts embedded will be discussed.

3.2.3.1 Some contacts embedded

In case of partial contacts (real or virtual) embedded in the substrate, the impedance extraction process is similar with the case of all contacts on the top surface of substrate, which has been discussed above.

The schematic for one contact embedded in a three layers substrate is shown as Figure 3-5.

Compare with the Figure 3-4, the boundary condition is the same, i.e. I_{out}=0 and I_1=1. Due to the contact B isn't located on the top surface, what we need to know is not the voltage V_1 as the model in Figure 3-4 but the correspondent voltage V_3 in Figure 3-5..

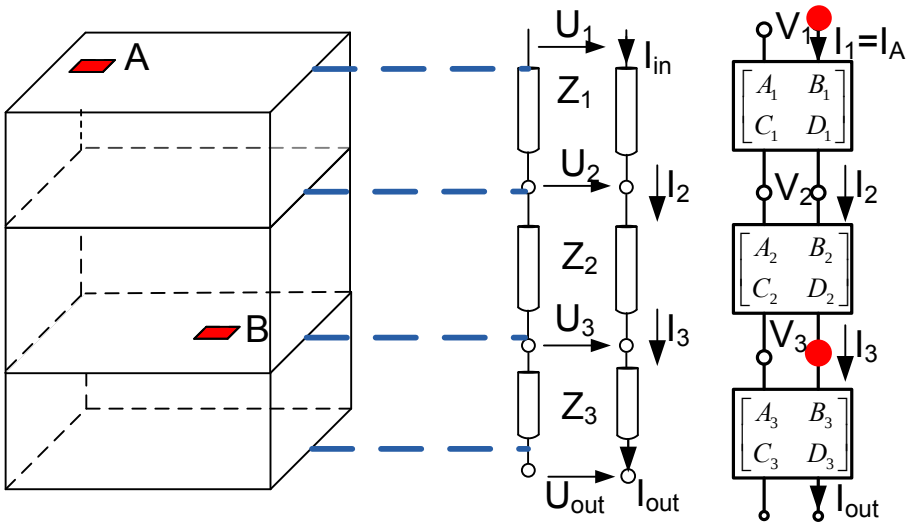


Figure 3-5 Model for some contacts embedded

As long as we get the ABCD parameter for each layer, the V_3 could be gotten easily under the condition of $I_{out}=0$ and $I_1=1$. Then Z_{31} is calculated by V_3 and I_1.

Replace Z_{11} by Z_{31} in equation(3.32) to calculate the spatial-frequency domain potential $\Phi(k_x,k_y,z=0)$. An inverse bi-dimensional spatial Fourier transform is applied to $\Phi(k_x,k_y,z=0)$ to get the potential distribution (φ_z) of the x-y plane which the contact B laid on. Then, equation(3.1) is applied to calculate Z_{BA}. The others Z parameter elements could be gotten similarly.

3.2.3.2 All contacts embedded

If all the contacts are embedded, the substrate can be seen as a parallel connection of two separate parts as shown in Figure 3-6.

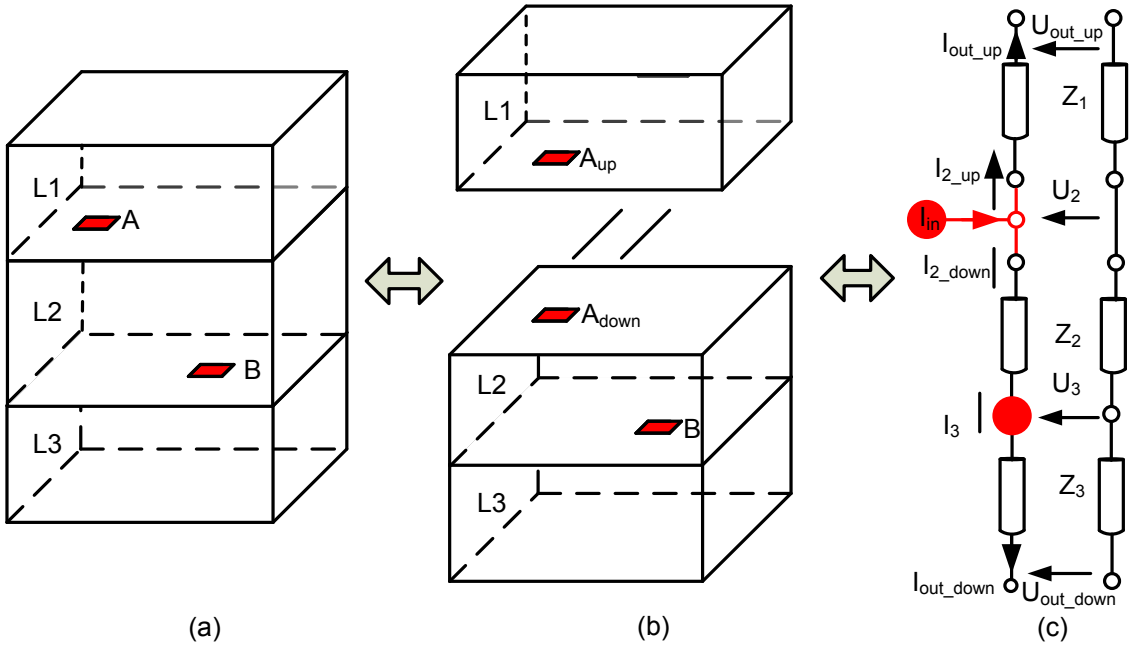


Figure 3-6 All contacts embedded model

The current is injected on contact A, so the substrate is divided to two parts, from the layer where A laid on (Figure 3-6 (b)). The equivalent TLM model is as shown in Figure 3-6 (c). The I_{out_up} and I_{out_down} are all zero due to the boundary condition[104]. I_{in} is unit current so I_{in}=1. In order to get the Z_{32}, what needs to know is the voltage $V_{3.}$ For the upper half substrate TLM model, assume the input impedance is Z_{in_up} and the bottom half one is the Z_{in_down}, due to the parallel connection we should have,

$$I_{2\_down} = I_{in} \frac{Z_{in\_up}}{Z_{in\_up} + Z_{in\_down}} \tag{3.38}$$

The Z_{in_up} and Z_{in_down} impedances can be calculated by the ABCD parameter of every layer as shown in Figure 3-6 (c). As one calculates the I_{2_down} the model will become exactly the same model as in Figure 3-5. The following steps are exactly the same with the partial contacts embedded model.

Use this method each layer's potential can be calculated. Figure 3-7 shows the potential of a substrate with two contacts one in layer 6 and the other in layer 9.

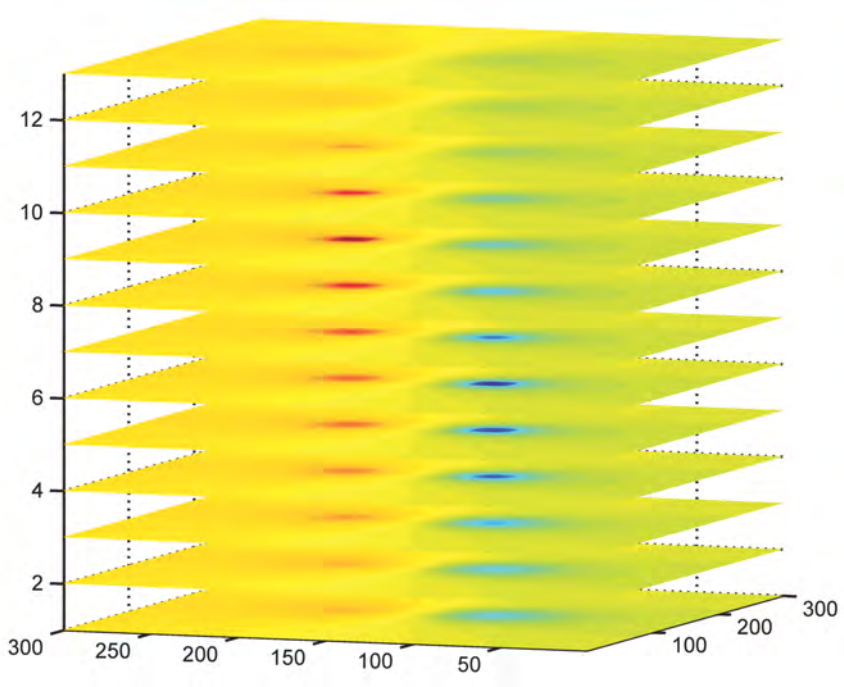


Figure 3-7 Potential of every layer of model for two contacts on Layer 6(Blue) and Layer 9(Red)

3.2.4 Impedance between Contacts and TSVs

Using our above analysis, one can calculate the impedance between any contacts laying on arbitrary locations and arbitrary layers. So, in order to calculate the impedance from TSV, considers a special structure as shown in Figure 3-8(a).

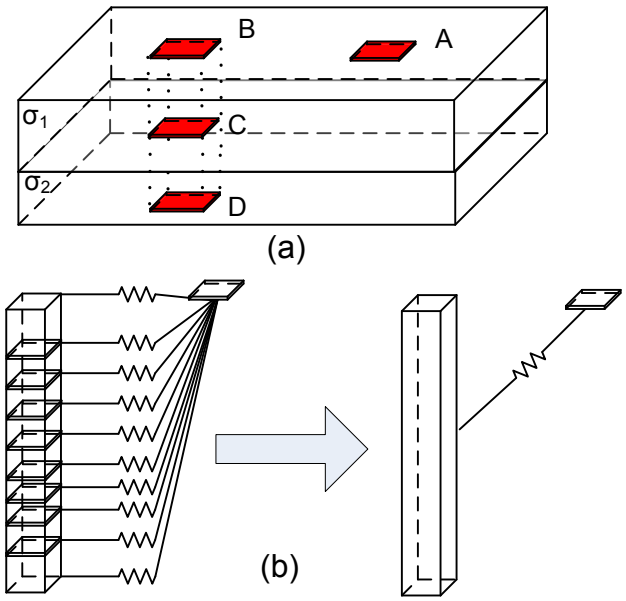


Figure 3-8 TSV-contacts equivalent model

The impedance between AB AC and AD could be calculated by the above algorithm. Then, we combine the coupling between AB AC and AD to get a coupling between contact A and "contact" BCD. Actually, the "contact BCD", the combination of B, C and D, is the TSV (Here we assume the TSV is not surrounded by oxide coating, the case of the TSV with oxide coating will be discussed later). A schematic is shown in Figure 3-8 (b).

One can divide the TSV into small parts, and then consider each part as a contact and use the above process to get the impedance between each small TSV part and the contacts. At last, combine all the impedance together to get the final impedance between the TSV and the contact as shown in Figure 3-8 (b).

Using a similar algorithm, the impedance between TSV and TSV could be calculated by dividing both TSV into small pieces. After getting the impedance between each "pieces" and the other TSV using method last section, the total impedance between 2 TSV could be gotten combining all the impedance.

3.2.5 Algorithm summary

So the general process of the algorithm can be expressed as following figure.

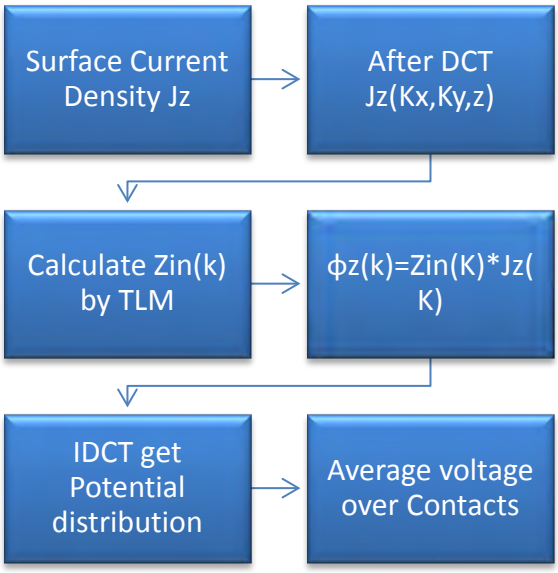


Figure 3-9 General steps of 3D IE algorithm

3.3 Model Validation

Now we can calculate, any impedance between contacts possibly embedded in the substrate, contacts can be introduced into any layer; they can be real (metal like) or virtual. In this section, a Z parameter of a multi-layers substrate will be extracted by 3D-IE and simulation method respectively.

Firstly, the impedance will be calculated exactly by our above algorithm. For the numerical simulation, we use COMSOL, a well known Multiphysics (electrical, thermal, stress couplings) simulator[104]; it is also a dedicated tool for full wave electromagnetic analysis. It uses essentially Galerkin-like algorithms[111]. Typically, a 3D simulation can use a few ten of minutes or hours.

In COMSOL, the boundary condition of the side surface and bottom surface is set as $\partial\vec{E}/\partial\vec{n}=0$. Inject a unit current to one contact and calculate the potential difference between two contacts to get the impedance between them.

In our TLM method, since, we inject a constant current density at any calculation point at the contact level, we use Millman's theorem[112] which is applied all over the contact. The contact voltage is the mean value of the voltage of the discrete contact element, calculated via Millman's theorem, as:

$$V=\frac{\sum_{n=1}^{N} j\omega c\varphi_n}{\sum_{n=1}^{N} j\omega c}=\frac{1}{N}\sum_{n=1}^{N}\varphi_n \qquad (3.39)$$

where φ_n is the substrate voltage at a node and N is the number of the coupled area is discredited. So the substrate plate is considered as a constant current density injection not a uniform potential.

We are very aware that the quasi-electrostatic modeling framework cannot work so perfectly up to 10THz (versus experiments), which implies a wave length of roughly ten um in Si; this wave length is of the same order of the contact-to-contact distance. Currently, we did not take into account explicitly the permeability; it is not realistic to go beyond 200GHz in this analysis (that is not so bad); but we think it was interesting comparing the element finite method to test the robustness of our algorithm.

The geometry schematic of the substrate doping to be tested is shown as in Figure 3-4(a). For the physic property, a p+/p region of interest of a 0.35μm process[113-115] is selected and decomposed in twelve layers from bottom to top with thicknesses of t1, t2...t12 and conductivities of σ1, σ2…σ12 which are as shown in Figure 3-10 and Figure 3-13. All layers' relative permittivity is 11.9.

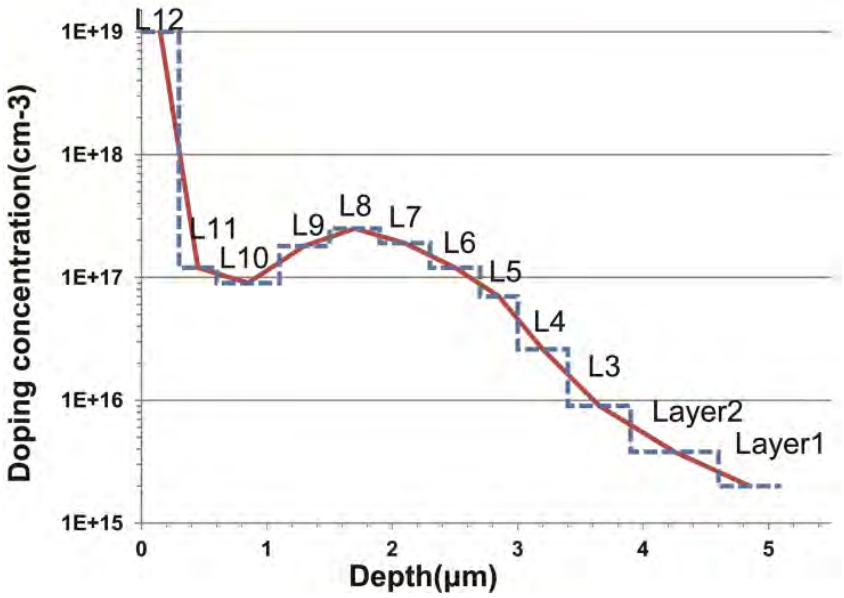


Figure 3-10 A specific depth profile of a 0.35μm technology (p- region)

The frequency characteristic of the impedance will be researched under the frequency from 10^8Hz to 10^{13}Hz and the separate distance in X direction between contacts (or TSVs) vary from 1μm to 16 μm.

3.3.1 Contacts on top surface

For a structure in Figure 3-4 (a), set the distance d between two contacts edge as 6μm; the impedance frequency characteristic extracted by proposal method and COMSOL are both shown in Figure 3-11(a). We can verify that the impedance decrease with the increase of frequency and the calculate results from our proposal method agree well with the COMSOL ones.

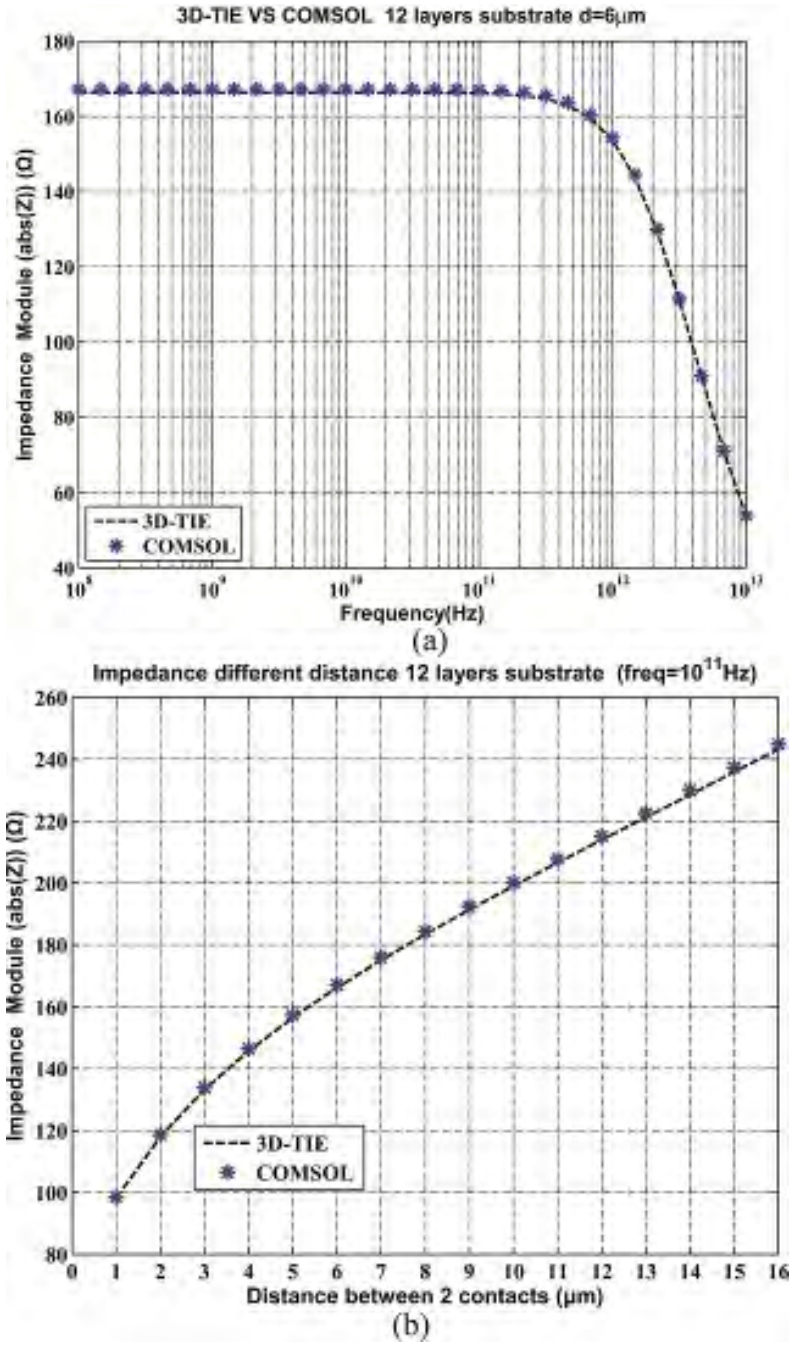


Figure 3-11 (a) Impedance for 12 layers substrate with separate distance d=6μm for two contacts which laid on top surface. The results are the impedance module. (b) Impedance for variable contacts separation 3D-IE vs. COMSOL. The results are under frequency equal

Use the same structure as in Figure 3-4 (a) to test the layout characteristic for two top surface contacts. Fix the frequency at 1e11Hz while varying the separate distance (d in Figure 3-4 (a)) of the two contacts from 1μm to 16 μm by step of 1μm. The resulting impedance modules are indicated in Figure 3-11(b). From the figure we can see the impedance increase with the raise of the distance between two contacts both in 3D-IE result and the COMSOL one.

Figure 3-12 gives the top surface potential distribution of a specific example at frequency=10^{11}Hz calculated by 3D-IE and COMSOL and they also show a good accord to each other.

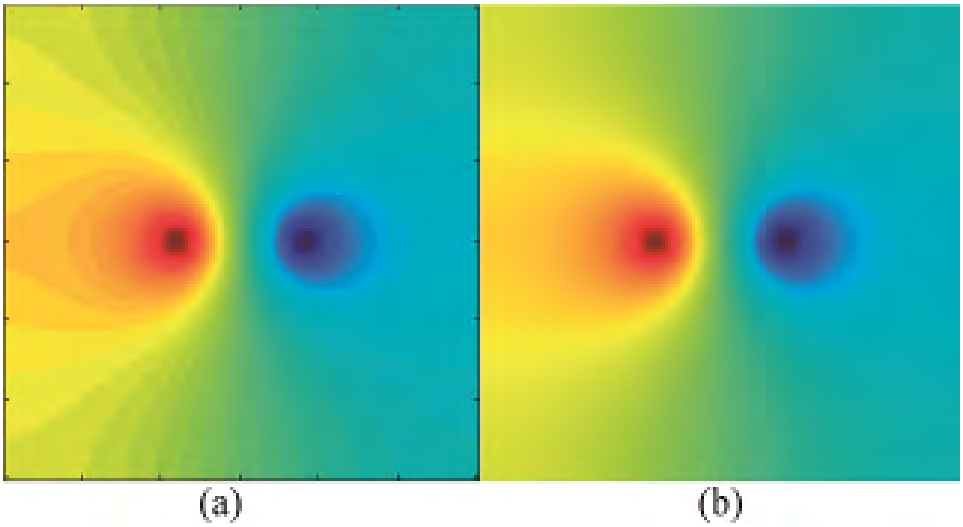


Figure 3-12 Top surface potential from 3D-IE(a) and COMSOL(b) for 12 layers substrate under dx=6μm and frequency=100GHz very good fits between FEM and TLM. Calculations are made with current source, then, we get voltage variation under contacts.

From above results one can find that the comparison between "TLM/Green" and "COMSOL" is quite good, proposal method calculate results agree well with the COMSOL simulation ones while proposal method use much less time.

Regard the top surface potential distribution of the two contacts model in Figure 3-12, one can find the potential on the contact surface are not uniform (high voltage region). The no uniform potential is caused by an injection of uniform current density instead of a uniform voltage. This no uniform potential feature makes 3D-IE very profitable when one calculates the impedance of two resistive regions rather than two metal contacts, for example, the oxide-insulated conductive regions (e.g. pads and coplanar waveguide) and junction-insulated well regions (e.g. n-well regions over a p-type substrate). In these cases, the substrate plates could not be considered as equipotential plate.

3.3.2 All contacts embedded

Then we embed the two contacts into the substrate. The substrate geometry and physic features keep still as the one in last test but with two contacts embedded as shown in Figure 3-13.

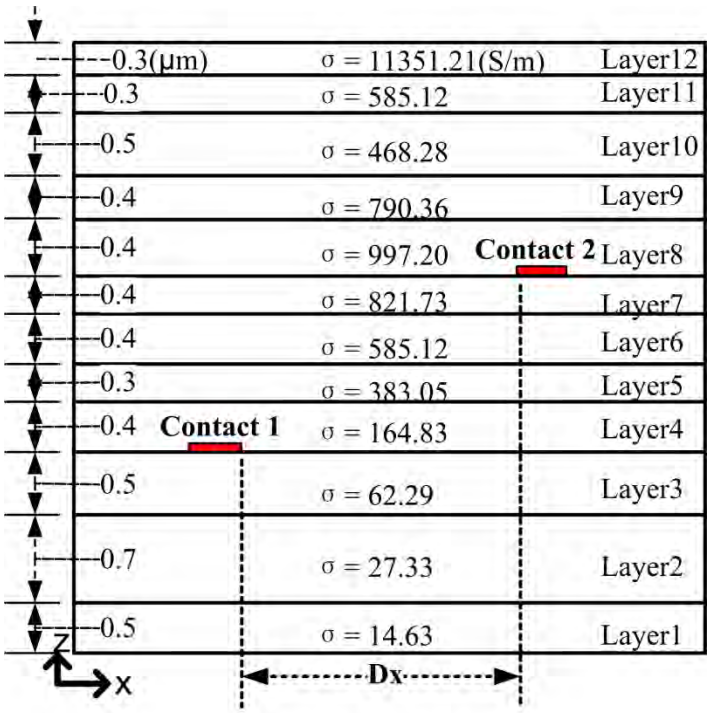


Figure 3-13 Substrate geometry feature in Z direction (thickness) and physic property (conductivity) with two embedded contacts, all the relative permittivity is 11.9. Embedded contacts laid in layer 4 and layer 8. The dimensions in X and Y direction for substrate and contacts are the same as in Figure 3-4(a)

One contact is embedded in the bottom surface of layer 4 and the other one is on bottom surface of layer 8. As above test for top surface contacts, the separate distance is set as 6μm and frequency from 1e8 to 1e13Hz. In order to analysis, two different COMSOL port setting are applied, constant current density (Constant CD) which inject a uniform current density to the contact port and constant voltage (Constant V) which inject a uniform voltage to the contact. The frequency results from these three methods are show in Figure 3-14(a). From results in Figure 3-14 (a), one finds a good fit of frequency characteristics for proposal method and COMSOL Constant CD one.

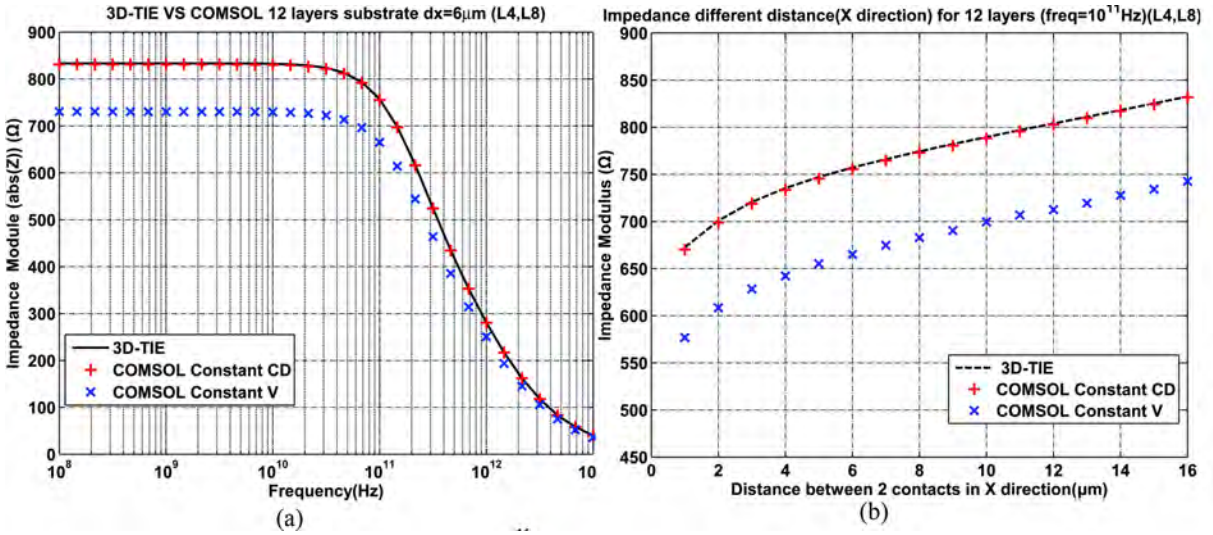


Figure 3-14 Impedance for 12 layers substrate with separate distance d=6μm for two contacts which are embedded in substrate. One is in layer 4 and the other one in layer 8. The results are the impedance module. (b) Impedance from different embedded contacts separation.

Figure 3-14 (b) depicts the impedance results under different separate distance with frequency equals 1e11Hz.

The potential distribution of the top surface of the substrate is presented in Figure 3-15. The results from 3D-IE and COMSOL agree very well with each other.

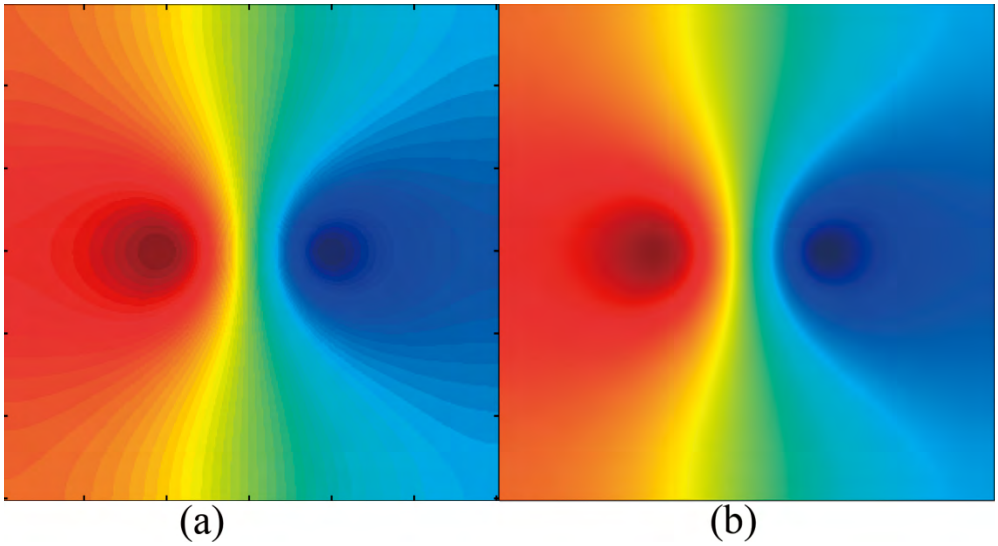


Figure 3-15 Substrate top surface potential which are gotten from 3D-IE (a) vs. COMSOL (b) for contacts embedded in 12 layers substrate in layer 4 and layer 8.

3.3.3 Impedance between contacts and TSVs

3.3.3.1 Contact-TSV

Based on the model of Figure 3-4 (a), one extrudes one of the contacts into the substrate to get a TSV of 5.1μm which occupies from layer 12 to layer 1; the contact-TSV model shown in Figure 3-16(a). The physic properties and thickness of every substrate layers of substrate keep still with Figure 3-13.

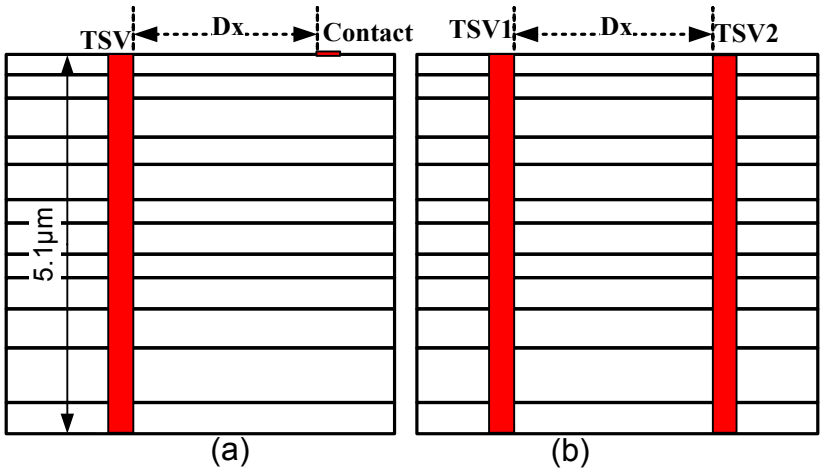


Figure 3-16 Schematic and property of TSV-Contact model (a) and TSV-TSV model (b). The TSV is gotten by extruding contact in Figure 3-4. The substrate dimension and physical property keep still as in Figure 3-13. The dimension of the TSV is 2μm×2μm×5.1μm in X, Y and Z direction

In the same research way, firstly, the separate distance is set to 6μm and frequency varies the frequency from 1e8 to 1e13Hz. Results in Figure 3-17(a) and Figure 3-17(b) show good fits of frequency characteristics for proposal method and COMSOL one in resistance and reactance respectively. The method "New Material" COMSOL can actually be considered as an anisotropic conductivity; this new material of via has the same conductivity as that of

copper in the Z direction, but the conductivity of the layers of the Si substrate in the X and Y directions (in our analytical method, actually, we do have lateral conductivities for the via: σ_{si}). In fact in the directions x, y, there is the capacitive effect of the oxide, but also a possible depleted area adjacent to the silicon oxide layer, and so much more as doping is low. While the classical method, COMSOL takes, in turn, for the TSV, an isotropic conductivity, here that of copper (default $\varepsilon_{Cu}=\varepsilon_0$). Ultimately, we should take into account these aspects more precisely.

Secondly, change the separate distance (Dx in Figure 3-16(a)) from 1μm to 16 μm under frequency equal 1e8Hz and test the impedance between TSV and contact. The anisotropy conductivity material is also used for comparing. Figure 3-17(c) shows a good accordance between our proposal method and the simulation one in the layout impedance feature. Figure 3-18 presents the potential of the TSV and contacts of COMSOL use the anisotropy material.

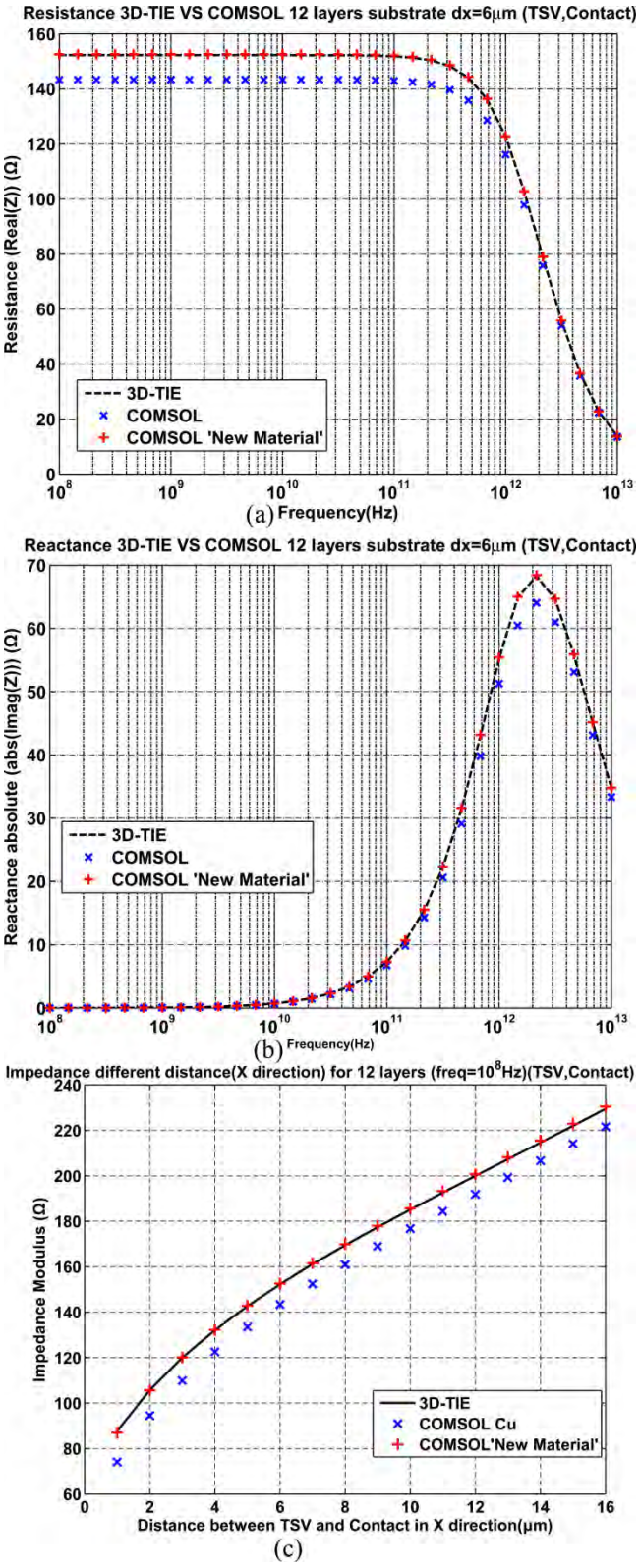


Figure 3-17 Resistance (a) and reactance absolute value (b) from 3D-IE and COMSOL between TSV and contact dx=6μm under frequency from 1e8Hz to 1e13Hz. The COMSOL "New Material" method is actually a COMSOL simulation results under an anisotropy conductivity TSV material. This material has the same conductivity with copper in Z direction but has the same conductivity with the substrate layers in X and Y direction. (c) Impedance from different TSV contacts separation 3D-TIE vs. COMSOL under freq=0.1GHz.

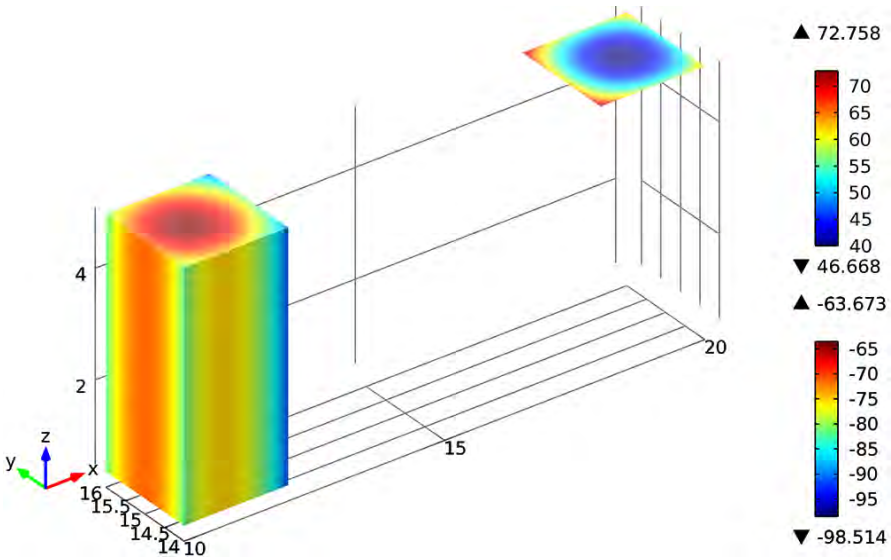


Figure 3-18 Potential of TSV-contact model with a TSV in an anisotropic material in which has the same conductivity component as copper in Z direction and has the same conductivity component as the silicon substrate in X and Y direction.

3.3.3.2 TSV-TSV

Based on contact-TSV model, extrude both contacts to get two TSVs which occupy from layer 13 to layer 1. Then a TSV-TSV model is built and its cross-section drawn is shown in Figure 3-16 (b).

Set the separate distance to 6μm, the frequency characteristic from 10^8Hz to 10^{13}Hz is shown in Figure 3-19(a). And then set the frequency as 1e8Hz, change the separate distance between two TSVs from 1μm to 16μm and extract the impedance between two TSVs. The two TSVs impedance extraction results for different separate distance under frequency 1e8Hz from COMSOL and 3D-IE are shown Figure 3-19(b).

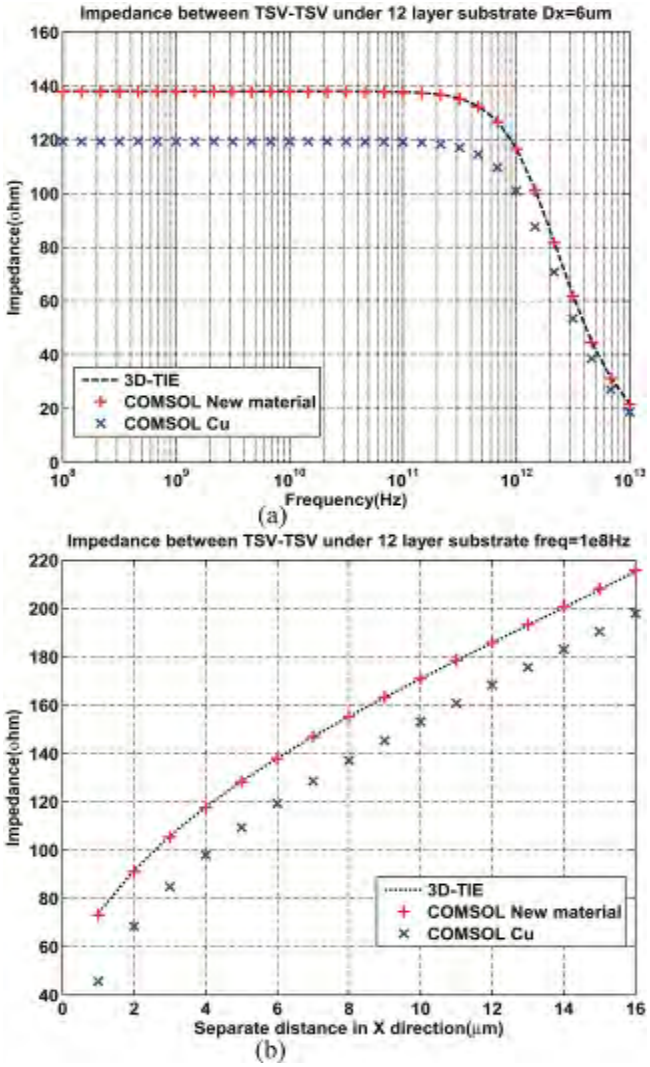


Figure 3-19 (a) Impedance module from 3D-IE and COMSOL between TSVs with Dx=6μm (b) Impedance from different TSVs separation 3D-IE vs. COMSOL

3.4 Improved model

3.4.1 Add oxide coating to TSV

In practice, the TSV has an oxide coating, for isolation; so an improved model is proposed as Figure 3-20.

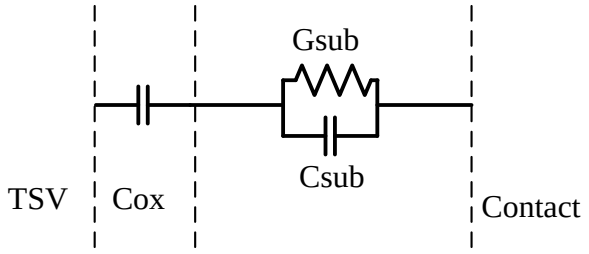


Figure 3-20 New equivalent model of coupling between TSV and contact

And comparing with the schematic in Figure 3-8(b), a capacitance effect is added to each pieces of the TSV between them and contact as shown in Figure 3-21.

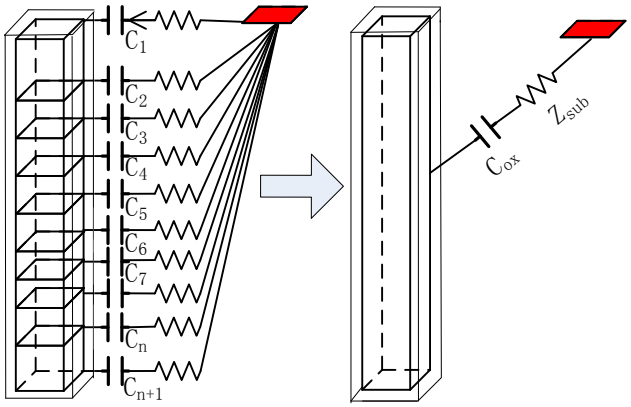


Figure 3-21 Schematic for TSV-contact model in which TSV is with oxide coating. Cox is the capacitance of the oxide coating surrounding the TSV; Zsub is the impedance of the substrate.

So the investigate step is, firstly, calculate the capacitance caused by the oxide layer; secondly, insert them appropriately into the model. The following sections will discuss these steps respectively.

3.4.1.1 Calculation of capacitance

Two different coating outside the TSV are shown in Figure 3-22. The fringing field[116] should be considered to get the accurate capacitance.[117] And approximately, they can also be calculated by the following formulas[118]. For the column one shown in the right of Figure 3-22, its capacitance can be calculated by equation(3.40).

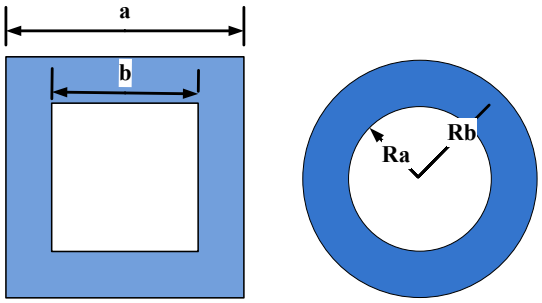


Figure 3-22Cross-section of two different oxide coatings outside two different types of TSV

$$C = \frac{8\varepsilon L}{\ln \frac{a}{b}} \tag{3.40}$$

And for a cylinder oxide coating shown in Figure 3-22 (with a length of L), the equation is

$$C = \frac{2\pi\varepsilon_0 L}{\ln \frac{R_b}{R_a}} \tag{3.41}$$

3.4.1.2 Algorithm

After getting the oxide capacitance, the capacitance effect could be added in 3D-IE program automatically by our following algorithm.

In order to explain how it works, we assume a specific structure as in Figure 3-23.

The matrix G is the admittance matrix which is calculated by 3D-IE. In this specific structure, it has 8 rows and 8 columns due to we have 1 TSV and 7 contacts. If we get the G matrix for a system, we can get the impedance between any two nodes. So the question is how to deduce the new admittance matrix with inserting capacity Cox from the original admittance matrix of the system. The TSV is node 8 which the oxide (capacitance Cox) is added.

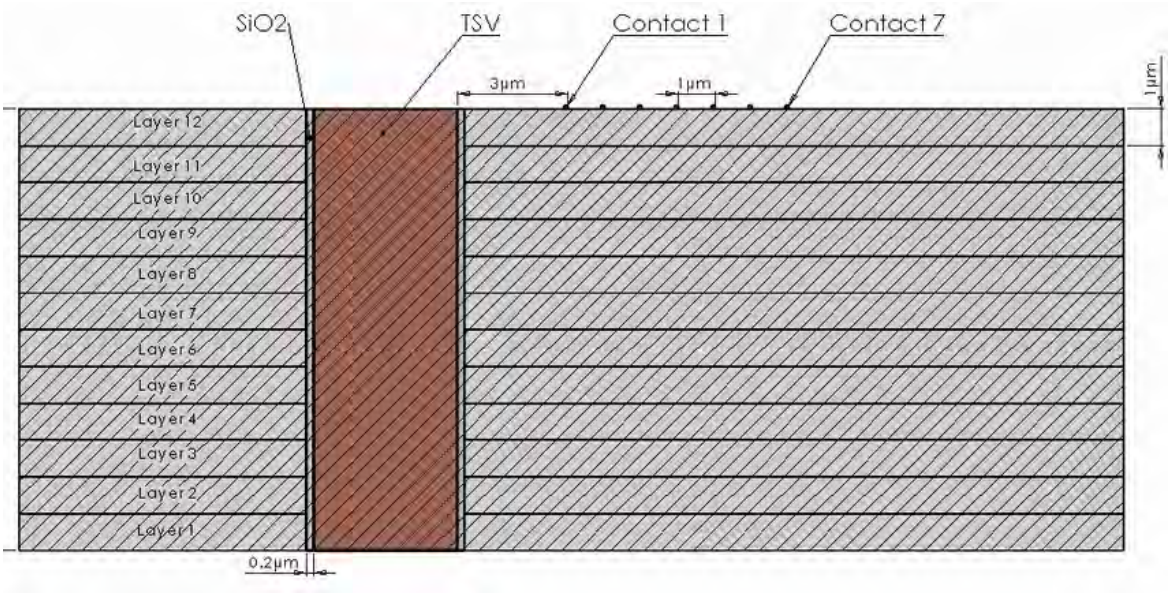


Figure 3-23 A specific structure with one TSV (with oxide layer) and 7 contacts

This is a structure with 1 TSV and 7 contacts. The TSV is surrounding by the oxide coating. The potential of every contact and TSV are defined by following figure.

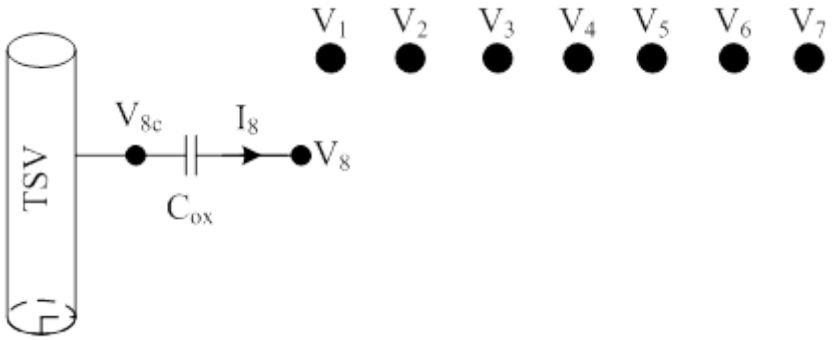


Figure 3-24 Abstract model for 1 TSV and 7 contacts

The potential of contacts are V_1 to V_7 and the outside surface potential of TSV coating is V_8 and inside the oxide coating is V_{8c}. Without oxide coating, V_{8c} should equal to V_8.

Before adding the oxide coating we have:

$$[I]=[G][V] \tag{3.42}$$

i.e.

$$\begin{bmatrix} I_1 \\ \vdots \\ I_8 \end{bmatrix} = \begin{bmatrix} G_{11} & \cdots & G_{18} \\ \vdots & \ddots & \vdots \\ G_{81} & \cdots & G_{88} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_8 \end{bmatrix} \tag{3.43}$$

And after adding oxide coating, the potential changed but the current keep the same value, so we should have

$$[I]=[G_c][V_c] \tag{3.44}$$

i.e.

$$\begin{bmatrix} I_1 \\ \vdots \\ I_8 \end{bmatrix}=\begin{bmatrix} G_{11c} & \cdots & G_{18c} \\ \vdots & \ddots & \vdots \\ G_{81c} & \cdots & G_{88c} \end{bmatrix}\begin{bmatrix} V_{1c} \\ \vdots \\ V_{8c} \end{bmatrix} \tag{3.45}$$

From Figure 3-24, $I_8=\dfrac{V_{8c}-V_8}{Z_s}$ where $Z_s=\dfrac{1}{j\omega c}$

So,

$$V_8=V_{8c}-I_8Z_s \tag{3.46}$$

From equation(3.43),

$$\begin{aligned} I_8 &= G_{81}V_1+G_{82}V_2+\cdots+G_{88}V_8 \\ &= G_{81}V_1+G_{82}V_2+\cdots+G_{88}(V_{8c}-I_8Z_s) \\ &= G_{81}V_1+G_{82}V_2+\cdots+G_{88}V_{8c}-G_{88}I_8Z_s \end{aligned} \tag{3.47}$$

So,

$$\begin{aligned} I_8+G_{88}I_8Z_s &= G_{81}V_1+G_{82}V_2+\cdots+G_{88}V_{8c} \\ I_8(1+G_{88}Z_s) &= G_{81}V_1+G_{82}V_2+\cdots+G_{88}V_{8c} \end{aligned}$$

$$I_8=\frac{1}{(1+G_{88}Z_s)}\left[G_{81}V_1+G_{82}V_2+\cdots+G_{88}V_{8c}\right] \tag{3.48}$$

Firstly, we deduce the reasoning formula for the first row of admittance matrix G.

From equation(3.43),

$$\begin{aligned} I_1 &= G_{11}V_1+G_{12}V_2+\cdots+G_{18}V_8 \\ &= G_{11}V_1+G_{12}V_2+\cdots+G_{18}(V_{8c}-I_8Z_s) \\ &= G_{11}V_1+G_{12}V_2+\cdots+G_{18}V_{8c}-G_{18}I_8Z_s \end{aligned} \tag{3.49}$$

Substitute equation(3.48) into equation(3.49)

$$\begin{aligned} I_1 &= G_{11}V_1+G_{12}V_2+\cdots+G_{18}V_{8c}-G_{18}Z_s\left(\frac{1}{(1+G_{88}Z_s)}\left[G_{81}V_1+G_{82}V_2+\cdots+G_{88}V_{8c}\right]\right) \\ &= \left(G_{11}-\frac{1}{(1+G_{88}Z_s)}G_{18}G_{81}Z_s\right)V_1+\left(G_{12}-\frac{1}{(1+G_{88}Z_s)}G_{18}G_{82}Z_s\right)V_2+\cdots \\ &+\left(G_{18}-\frac{1}{(1+G_{88}Z_s)}G_{18}G_{88}Z_s\right)V_{8c} \end{aligned} \tag{3.50}$$

From equation(3.45),

$$I_1=G_{11c}V_{1c}+G_{12c}V_{2c}+\cdots+G_{18c}V_{8c} \tag{3.51}$$

In our specific structure, the oxide coating is only added to the TSV surface, so we still have $V_1 = V_{1c}, V_2 = V_{2c}, \cdots, V_7 = V_{7c}$. Compare above equation(3.50) and equation(3.51) one can get,

$$G_{1jc} = G_{1j} - \frac{1}{(1+G_{88}Z_s)} G_{18}G_{8j}Z_s, where(j = 1\cdots 8) \tag{3.52}$$

Secondly, we deduce the reasoning formula for the second row of admittance matrix G. Similarly, from equation(3.43),

$$\begin{aligned} I_2 &= G_{21}V_1 + G_{22}V_2 + \cdots + G_{28}V_8 \\ &= G_{21}V_1 + G_{22}V_2 + \cdots + G_{28}(V_{8c} - I_8 Z_s) \\ &= G_{21}V_1 + G_{22}V_2 + \cdots + G_{28}V_{8c} - G_{28}I_8 Z_s \end{aligned} \tag{3.53}$$

Substitute equation(3.48) into equation(3.53),

$$\begin{aligned} I_2 &= G_{21}V_1 + G_{22}V_2 + \cdots + G_{28}V_{8c} - G_{28}Z_s\left(\frac{1}{(1+G_{88}Z_s)}\left[G_{81}V_1 + G_{82}V_2 + \cdots + G_{88}V_{8c}\right]\right) \\ &= \left(G_{21} - \frac{1}{(1+G_{88}Z_s)}G_{28}G_{81}Z_s\right)V_1 + \\ &\left(G_{22} - \frac{1}{(1+G_{88}Z_s)}G_{28}G_{82}Z_s\right)V_2 + \cdots + \left(G_{28} - \frac{1}{(1+G_{88}Z_s)}G_{28}G_{88}Z_s\right)V_{8c} \end{aligned} \tag{3.54}$$

From equation(3.45),

$$I_2 = G_{21c}V_{1c} + G_{22c}V_{2c} + \cdots + G_{28c}V_{8c} \tag{3.55}$$

As before, $V_1 = V_{1c}, V_2 = V_{2c}, \cdots, V_7 = V_{7c}$. Compare equation(3.54) and equation(3.55),

So,

$$G_{2jc} = G_{2j} - \frac{1}{(1+G_{88}Z_s)}G_{28}G_{8j}Z_s, \text{where}(j = 1\cdots 8) \tag{3.56}$$

The step for deducing the formals for row 3 to row 7 are similar, now for row 8,

From equation(3.45),

$$I_8 = G_{81c}V_{1c} + G_{82c}V_{2c} + \cdots + G_{88c}V_{8c} \tag{3.57}$$

Due to $V_1 = V_{1c}, V_2 = V_{2c}, \cdots, V_7 = V_{7c}$, so equation(3.48) could rewrite as,

$$I_8 = \frac{1}{(1+G_{88}Z_s)}\left[G_{81}V_{1c} + G_{82}V_{2c} + \cdots + G_{88}V_{8c}\right] \tag{3.58}$$

Compare equation(3.57) and equation(3.58), one can get,

$$G_{81c} = \frac{1}{(1+G_{88}Z_s)}G_{81}, G_{82c} = \frac{1}{(1+G_{88}Z_s)}G_{82}, \cdots, G_{88c} = \frac{1}{(1+G_{88}Z_s)}G_{88} \tag{3.59}$$

So one has,

$$G_{8jc} = \frac{1}{(1+G_{88}Z_s)}G_{8j}, where(j = 1\cdots 8) \tag{3.60}$$

Equation(3.60) can also be written as

$$G_{8jc} = \frac{1}{(1+G_{88}Z_s)}G_{8j} = G_{8j}\left(1-\frac{G_{88}Z_s}{(1+G_{88}Z_s)}\right) = G_{8j} - \frac{1}{(1+G_{88}Z_s)}G_{88}G_{8j}Z_s \quad (3.61)$$

Combine equation(3.52), equation(3.56) and equation(3.61),

$$G_{ijc} = G_{ij} - \frac{1}{(1+G_{88}Z_s)}G_{i8}G_{8j}Z_s \quad (3.62)$$

In this specific structure the oxide capacitance Cox is add the node 8(TSV), if the oxide coating is added to the other nodes (ex. node m) of the structure, we can deduce the total inferential reasoning formula is:

$$G_{ijc} = G_{ij} - \frac{1}{(1+G_{mm}Z_s)}G_{im}G_{mj}Z_s \quad (3.63)$$

3.4.1.3 Model and verification

So from above discuss we can see, adding an oxide coating to a contact (or TSV) is only a transform of admittance matrix form G_{ij} to G_{ijc} using equation(3.63). After adding the oxide coating to the TSV, the new equivalent circuit between TSV and contacts is shown in Figure 3-25.

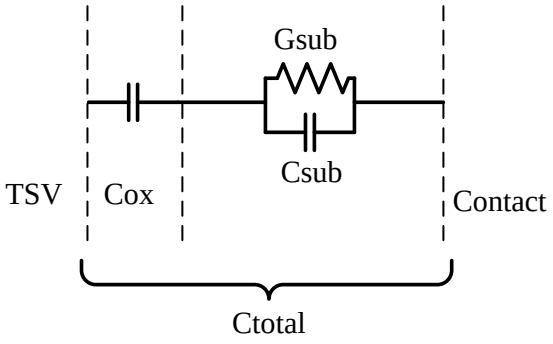


Figure 3-25 New model for the capacitance total between TSV and contact

In order to verification the result of our 3D-IE, a model is constructed in COMSOL as shown in following Figure 3-26, the blue coating outside the TSV is oxide layer. The distance between TSV and contact is 6μm. The TSV and contact is both square 2μm×2μm; thickness of oxide layer is 0.5μm outside TSV. The substrate structure and property is the same as before.

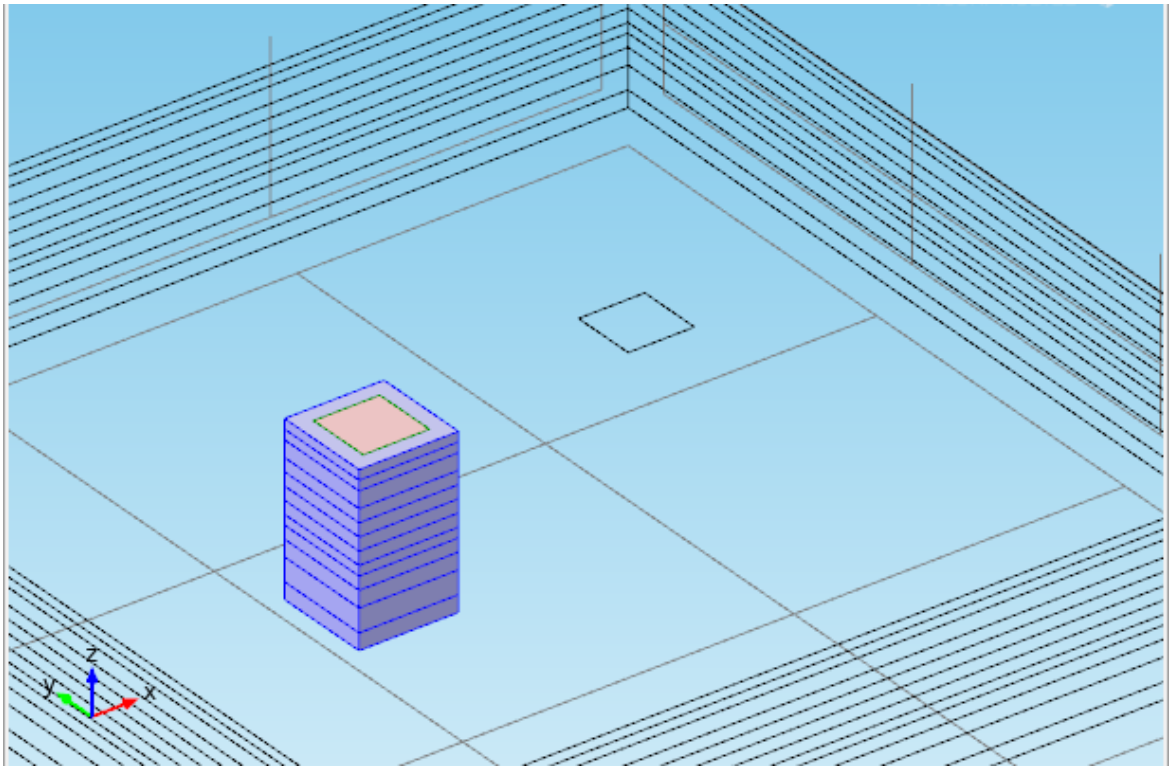


Figure 3-26 Model for verification of adding oxide coating

As shown in Figure 3-25, the total capacitance between TSV and contact is extracted by 3D-IE and COMSOL separately. The C_{total} is a combination of the capacitance oxide C_{ox} and capacitance substrate $C_{sub.}$

In 3D-IE, two different methods are used,

A) Treat the TSV as a combination of some pieces and add Cox to each part of the TSV;

B) Combine all the TSV parts to be a whole TSV and add a Cox totally directly.

The results of Ctotal calculated by 3D-IE and COMSOL are shown in Figure 3-27.

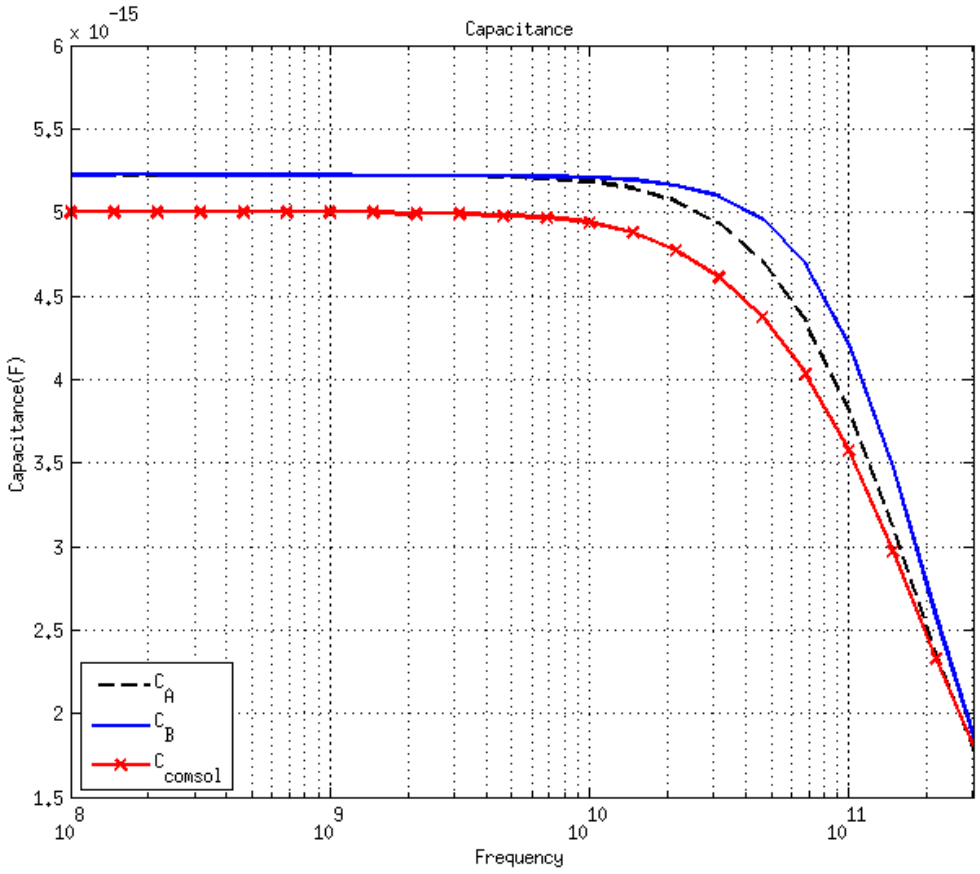


Figure 3-27 Comparison the equivalent capacitance from 3D IE and COMSOL

From above figure one can find, compared with the result of COMSOL, method A is more accurate in high frequency than method B but they present both a lack of accuracy.

One possible explanation maybe is the depletion region[119] capacitance which is in series with the capacitance oxide.

"The depletion region is also called depletion layer, depletion zone, junction region or the space charge region, is an insulating region within a conductive, doped semiconductor material where the mobile charge carriers have diffused away, or have been forced away by an electric field. The only elements left in the depletion region are ionized donor or acceptor impurities." [120]

A full derivation steps for the depletion width could be found in [121]. The derivation is based on solving the Poisson equation.

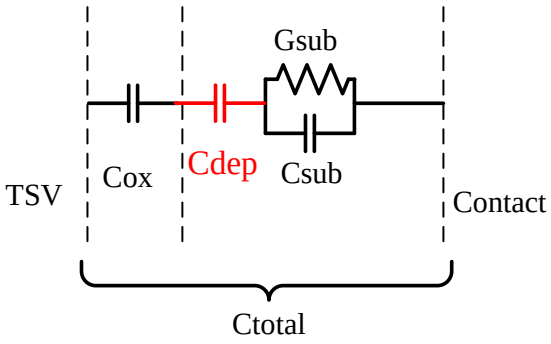


Figure 3-28 A possible model for the substrate with depletion region

To go one step further, we extract scattering parameters of two via embedded in the substrate (Figure 3-16 (b)), where each "piece" of TSV is surrounded by a thin oxide/inducting same capacitance, with a RDL connecting them. Besides, this inter via line (RDL) between the two TSV can be modeled as an equivalent RL circuit, or RLC considering the oxide which surrounds it. Its resistance (R_{line}) and inductance (L_{line}) are calculated analytically and, regarding its weak dimensions, can be considered as constant with frequency, up to 20 GHz, we find, with a first draft, some good fits between experiments, numerical simulations and our analytical ones.

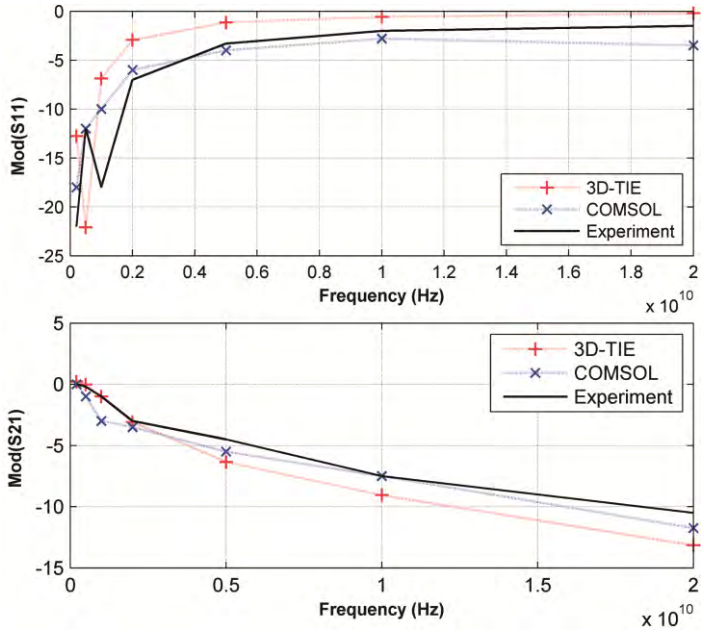


Figure 3-29 A first result from 3D-IE, COMSOL and experiment for a dual-TSV structure

Here our key goal is to explain our methodology; but we should consider, in future trends the capacitance not only induced by the coating oxide, but also by a depletion layer in series with this latter one, mainly for a low doped substrate; for instance, resolving Poisson's equation, in cylinder coordinates (in 2D, if the length of the via is very large compared to its diameter).

3.4.2 Alteration of shapes and numbers

Not like the other green function based method (c.f.[122]) which can only calculate the rectangle contacts, 3D-IE can be used the calculated to any shape. The circle, concentric circles, rectangle, loop, T-shape and so on. The following figure shows some examples of our 3D-IE. We will verify the result by comparing with the results from COMSOL.

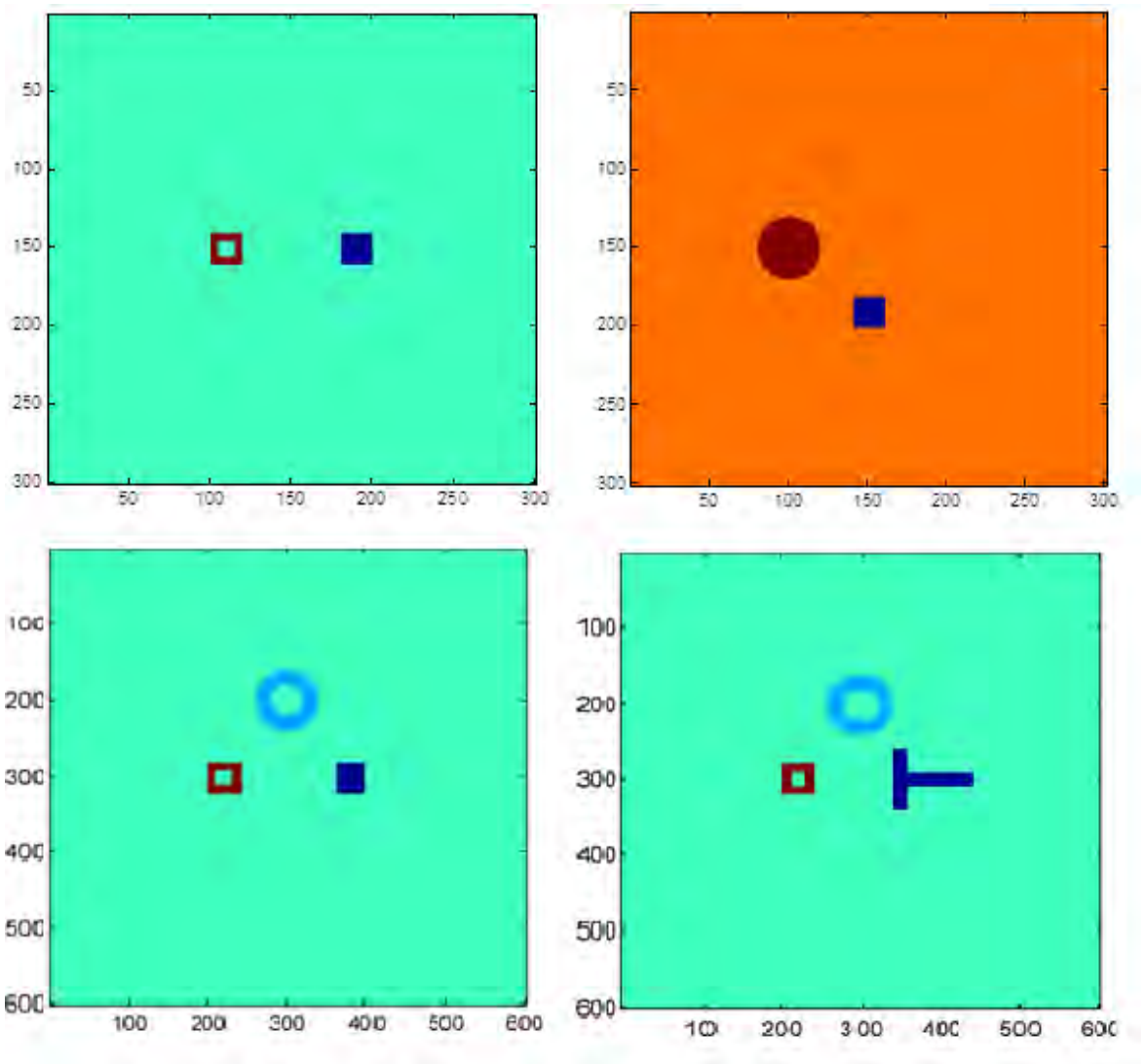


Figure 3-30 Different shape of contacts which can be calculated by 3D-IE

3.4.2.1 Model verification

Firstly, we do a model with 3 contracts on the top surface with three different shapes as the last one figure in Figure 3-30. The geometry details for the contacts locations and dimensions are as in following Figure 3-31.

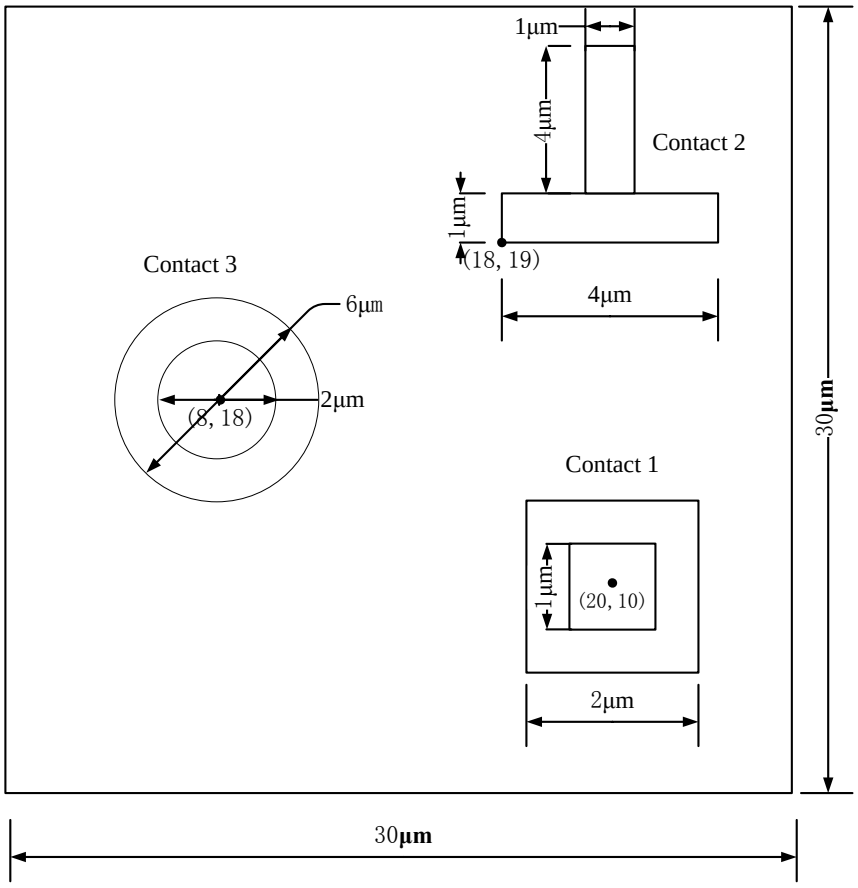
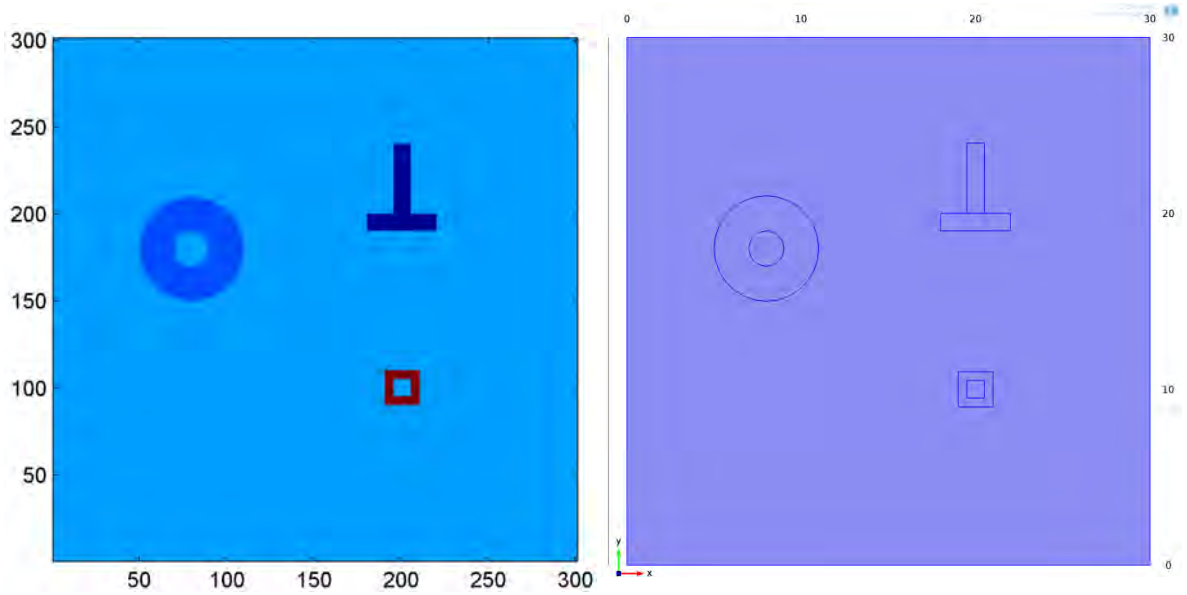


Figure 3-31 Geometry details for the contacts

The physic property of the substrate is the same as Figure 3-13. All the three contacts are on the top surface of the substrate. The screenshots from 3D-IE and COMSOL are shown as followed (Figure 3-32). The square contact is the contact 1, the T-shape contact is contact 2 and the circle one is contact 3.



(a) (b)

Figure 3-32 Screenshots for 3 contacts models from 3D-IE (a) and COMSOL (b)

The module of impedances between these 3 contacts calculated from 3D-IE and COMSOL are shown together in Figure 3-33, in which, the Z12 is the impedance between contact 1 and contact 2, the rest are in the similar manner.

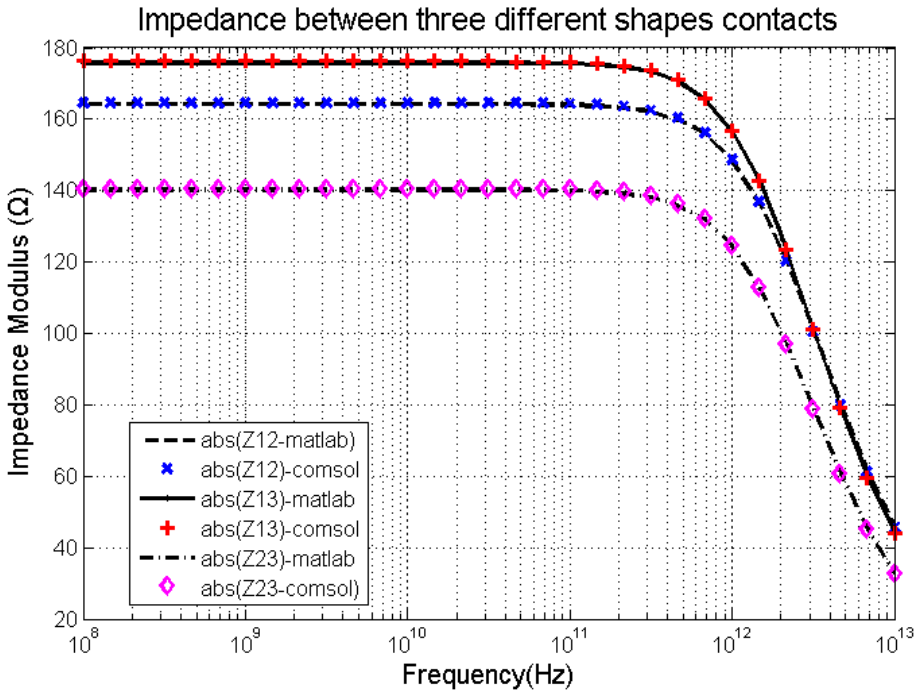


Figure 3-33 Impedance module for three different shapes contacts

From above figure we can see, the results from proposed methods agree very well with the results calculated from the COMSOL.

Then we test a model to verify the 3D-IE result compared with COMOSL for a new shape (not solid) TSV and contacts. In practice case, the TSV is not always solid block but sometimes with some insulation material filled in. So we do a specific TSV model as shown in Figure 3-34.

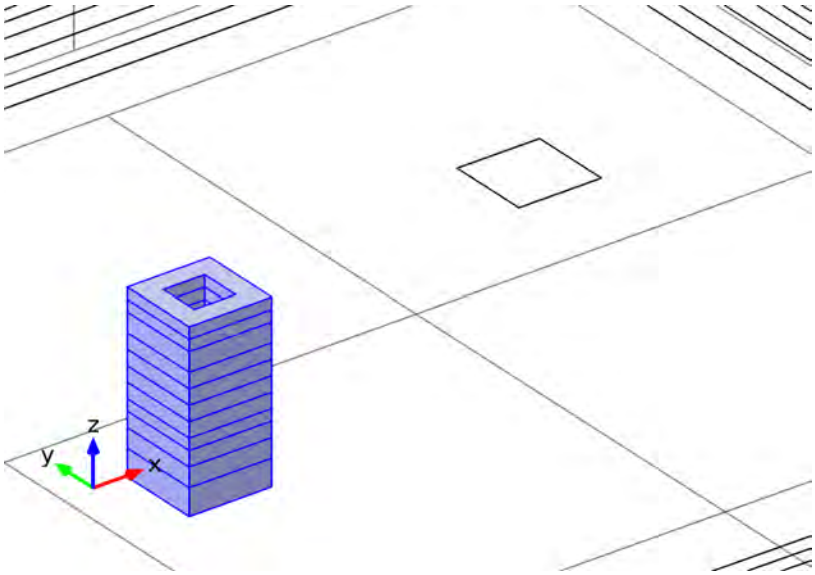


Figure 3-34 Loop TSV and contact

The thickness of the TSV is 0.5μm and the gap between TSV and contact is 6μm. The impedance module extracted by 3D-IE and COMSOL are shown in Figure 3-35.

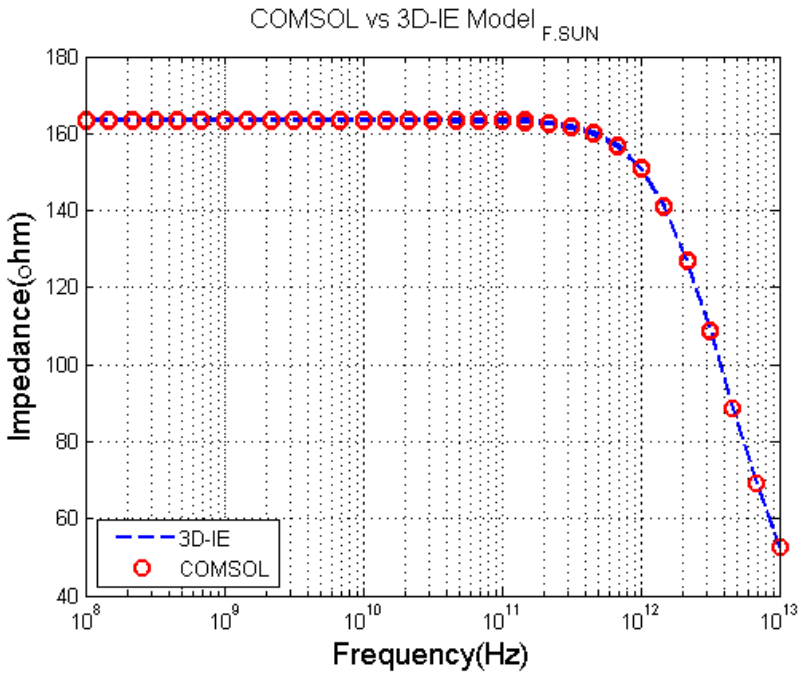


Figure 3-35 Impedance between a loop TSV and contact

Following figures show the top surface potential distribution for a 4μm TSV (thickness 0.5μm) from 3D-IE and COMSOL.

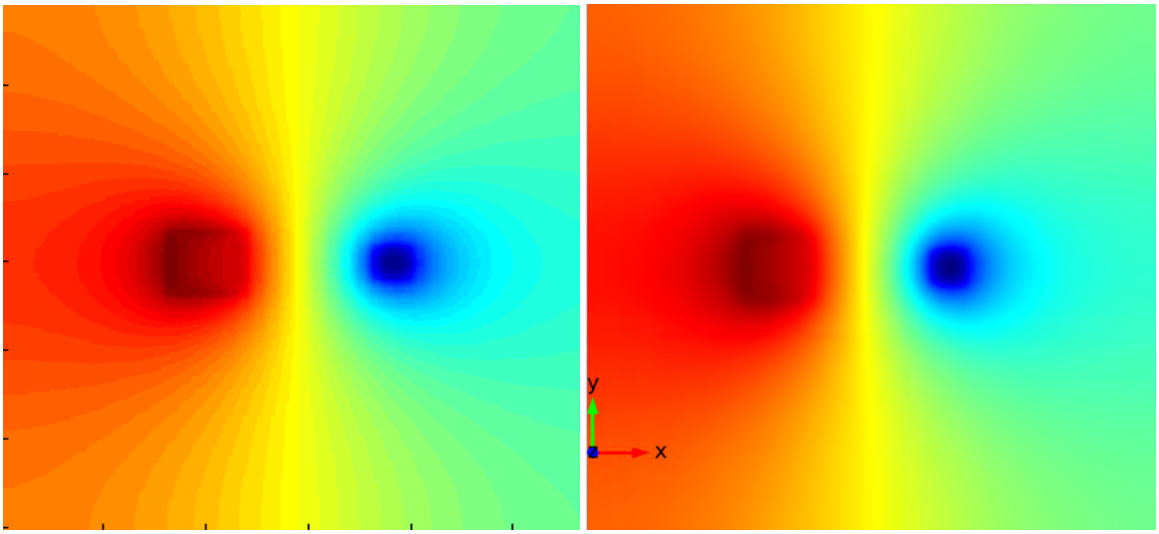


Figure 3-36 Potential distribution of the top surface

3.4.3 Lateral Permittivity Variation: possible method

If there are trenches and/or wells in a substrate, the layer's homogeneous assumption becomes disabled, and the Green function cannot be used directly. Traditional substrate coupling extraction based on Green function technique is limited to planar structures and it is usually difficult to develop analytical models for handling lateral variations in the dielectric constant.

A two-problem approach is proposed by Ranjit Gharpurey[122] and extended to three dimension by Chenggang Xu[123].

Firstly, we present how Gharpurey treat this. The boundaries can be considered as equipotential if the lateral variations are localized and small, otherwise it requires both

analytical and numerical techniques. An example of a large lateral variation can be a deep and wide oxide trench on the surface of the substrate, as some well. The algorithm of Gharpurey for solving this is explained by considering a specific schematic shown in Figure 3-37.

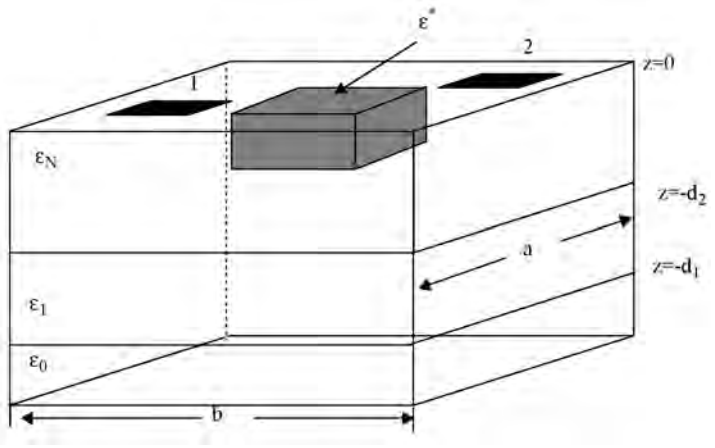


Figure 3-37 Lateral Variation in the Dielectric Constant[122]

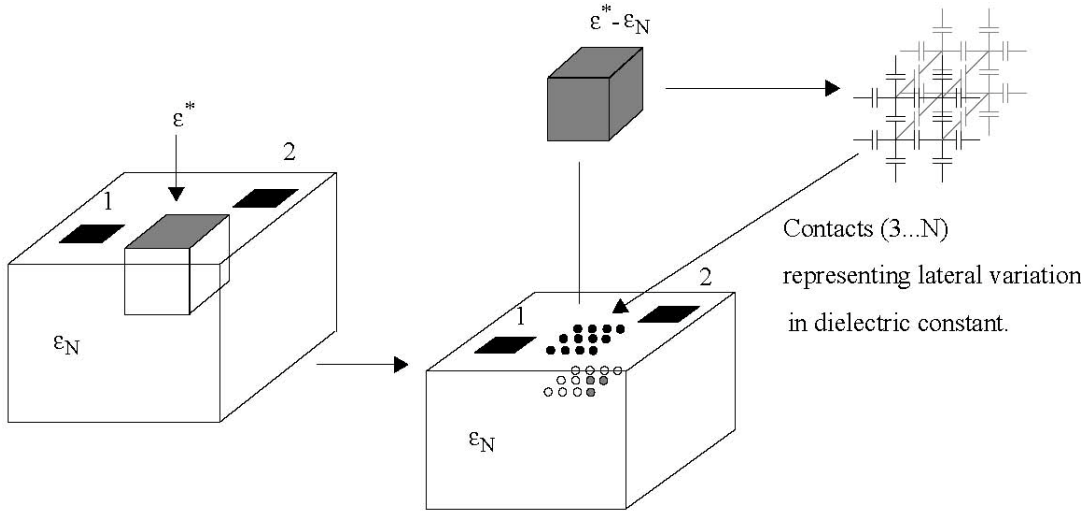


Figure 3-38 A Technique to Model Lateral Dielectric Constant Variations[122]

In Gharpurey's algorithm, the problem is considered to be a superposition of two problems as shown in Figure 3-38. The first problem consists of the original contacts and several equivalent contacts (3-N) in the region where the lateral variation in the dielectric constant was located. The dielectric constant of the entire top layer is assumed to be ε_n and the capacitance meshes for contacts 1-N are computed using the Green function technique. In the second problem the equivalent capacitance matrix for a material of dielectric constant $\varepsilon^*-\varepsilon_N$ is calculated. This is a simple grid representation of this material. This grid is then placed in parallel with contacts 3-N in the circuit simulator in order to compute the effect of the lateral variation in the dielectric constant.

And we find, if there are n region imbedded in each other (cf. Russian dolls), we can apply n times the superposition theorem. So Gharpurey's algorithm can be simply presented as in Figure 3-39.

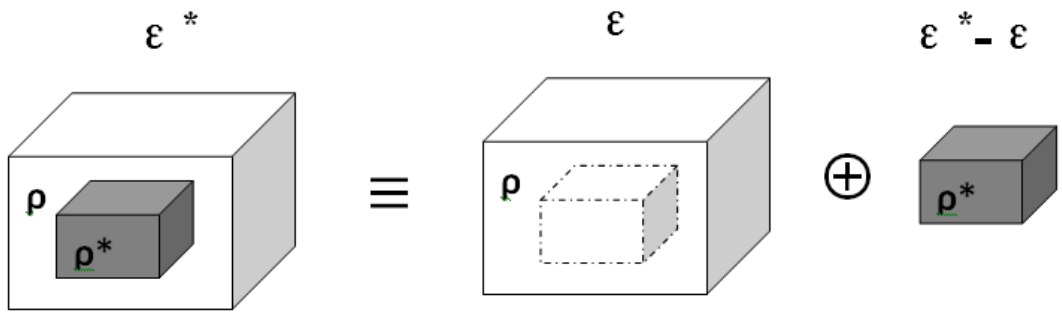


Figure 3-39 Lateral Variation in the Dielectric Constant

But Gharpurey's algorithm is only adapted to the two dimension contacts (since the contact thickness is usually much smaller than its lateral dimensions, contacts can be approximated as planar contacts in the x-y plane with zero thickness). So Xu extend this to three dimensions, which can be applied to 3D contacts as shown in Figure 3-40.

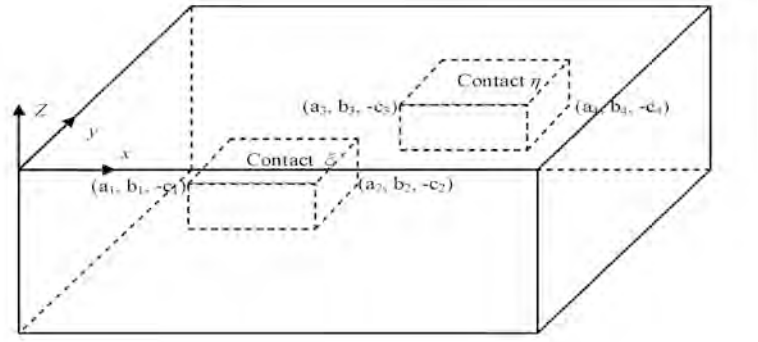


Figure 3-40 Definition of three-dimensional contacts[123]

The solution steps for Xu are presented as in Figure 3-41 which is similar with Gharpurey's.

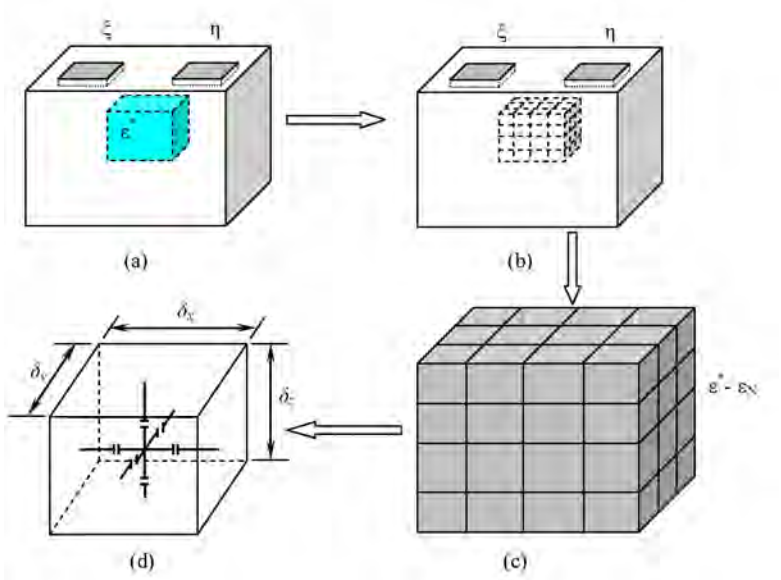


Figure 3-41 Schematic for the two-problem approach for lateral permittivity variation of Chenggang Xu[123]

In Gharpurey's method, the resultant network is included into a circuit simulator to compute the effect of the lateral permittivity variation, as suggested in[124]. However, this will increase the number of nodes in the simulation significantly and, therefore, may not be

computationally efficient. Xu gives a better way which is to lump the capacitance network to the real contacts. More details can be found in references [123, 125]

3.5 Conclusion and perspective

An efficient and perhaps elegant technique to model substrate coupling in 3D circuits, based on a transmission line algorithm, via frequency dependant impedance extraction, is presented and programmed. The technique uses a combination of the classical Green function or transmission line method approach and the use of Fast Fourier Transforms. The speed of this latter technique makes it suitable for optimization of circuit layout, for minimization of substrate coupling related effects. However, the earlier models are often limited to the surface contacts.

In practice, in this work, the contacts can be placed anywhere into the substrate; this is new, up to our knowledge. So, a new research should be enhanced for 3D. Besides, for contacts embedded in the substrate, we find some good fits between numerical simulations (FEM) and our analytical ones.

This technique could be used to embedded metal contacts or/and TSV. The speed of our proposed method is suitable for optimization of circuit layout, for minimization of substrate coupling related effects.

Further work will be developed, that will encompass accurate TSV models: skin and second order substrate effects, eddy currents, electromagnetic coupling between TSVs, in order to portray a more complete picture of the TSV-substrate interaction. This methodology could be extended to noise modeling, replacing small signals analysis by some stochastic fluctuations; calculations will be derived via a transfer impedance method, grasping noise at any probe into the substrate, from noise sources correlated (cf. nanoscale) or not.

4 3D-Interconnects Compact Models

4.1 Introduction

As stated in Chapters one and two, 2D planar technologies encounter many challenges, as a consequence, 3D integration is considered as a most promising solution. However, due to the high dense integration, 3D integration implies that the whole electrical context must be considered as current paths or couplings between chip elements. So, in order to accurately evaluating 3D system performances in design process, electrical compact models are notably required for 3D interconnects, including Through-Silicon Via.

In this chapter the compact models of 3D interconnect are presented, notably medium-density TSVs, reliable for low and medium frequencies (up to 20 GHz). 3D electromagnetic simulations and parametrical extractions are performed on test structures. The modeling approach that we propose is also presented in our submitted paper[126] which includes the consideration of the global electrical context. The substrate coupling extraction method from last chapter will be combined here to extract the accurate model. The proposed compact models and their respective analytical expressions; an illustration of the global electrical context in the cases of the presented test structures; and the substrate modeling approaches are dealt with. This extraction method is experimentally validated in the case of a coplanar waveguide atop a high-resistive substrate. The test structures' RF behaviors are also investigated. Finally, the conclusion summarizes the chapter's essential points and outlines on-going/future work.

4.1.1 The different steps of the modeling approach

3D interconnects necessitate the consideration of the global electrical context to correctly evaluate system performances. The compact models must hence be derived from semiconductor and electromagnetic theory instead of being developed and extracted outside of a realistic 3D IC system environment; the electrical models could be restrictive in this latter case by being only useful for specific applications. That is why the proposed compact models are in first instance based on parametrical extractions performed on test structures.

4.2 3D TSV Modeling with Global Electrical Context Consideration

4.2.1 Compact models of the medium-TSV and the coplanar line

Similar to 2D technologies, 3D interconnects can be built as RLCG equivalent electrical models described as Π or T networks. It does not matter which type of network as long as the interconnect length is smaller than the tenth of the propagated signal wavelength. Otherwise, the two networks do not have the same RF behavior and they must be distributed in a certain number of elementary cells to give equivalent responses. The T network will be considered later on in this chapter. Each of the 3D interconnect RLCG networks is modeled with serial elements (resistances and/or partial inductances) to model the signal propagation and parallel elements (capacitance and/or conductance) to model the interconnect environment. The proximity (or coupling) effects are also included in the compact model description. The geometrical parameters describing the analytical expressions are all expressed in meters. The coplanar line resistances and the self and mutual inductances are calculated from well-known formulae equation(4.1), (4.2) and (4.3). The resistances are calculated for a DC value (the skin effect could be easily considered) and the inductances are calculated depending on the partial inductance analytical expressions [127].

$$R = \rho \frac{L}{W \cdot T} \tag{4.1}$$

$$L_{self} = \mu_0 \mu_r \frac{L}{2\pi}\left[\ln\left(\frac{2L}{W+T}\right) + 0.5 + \frac{0.447(W+T)}{2L}\right] \tag{4.2}$$

$$M = \mu_0 \mu_r \frac{L}{2\pi}\left[\ln\left(\frac{2L}{p}\right) - 1 + \frac{p}{L}\right] \tag{4.3}$$

where ρ is the metal resistivity (copper: 1.72e-8 Ω•m); μ_0 and μ_r the vacuum and the copper permeability; *W, L, T* and *P* respectively the line width, length, thickness and the pitch between two interconnect lines (Figure 4-1).

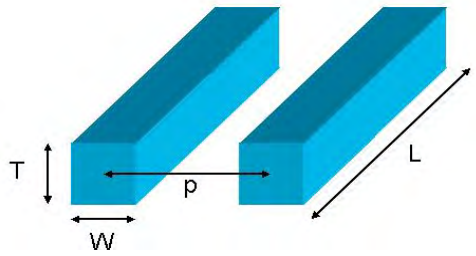


Figure 4-1 Schematic of the coplanar lines

The interline capacitance C_{inter} (or coupling capacitance) is calculated according to the set of equations defined in [128] from the concerned line surfaces, and the fringe capacitances taken at the extremities (*Cf)* and the middle (*Cf'*) of the coupled-line system. The electrical parameter *Cp* corresponds to the coupling capacitance between the ground plane and the line surface concerned (Figure 4-2); it is also referred to the literature as the line's self capacitance.

$$Cf = \varepsilon_0 \varepsilon_{ox} \left(0.075 \frac{W}{H} + 1.4 \left(\frac{T}{H} \right)^{0.222} \right) \tag{4.4}$$

$$Cf' = \frac{Cf}{1 + (H/S)} \tag{4.5}$$

$$Cp = \varepsilon_0 \varepsilon_{ox} \frac{W \cdot L}{H} \tag{4.6}$$

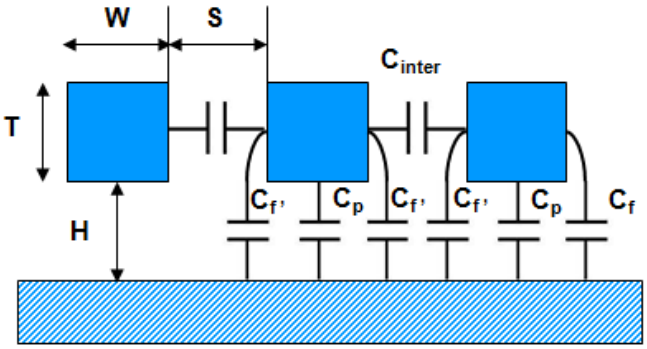


Figure 4-2 Illustration of the capacitive couplings between parallel lines located over a ground plane.

$$C_{inter} = Cf - Cf' + \frac{\varepsilon_0 \varepsilon_{ox} L}{100} \left(3 \frac{W}{H} + 83 \frac{T}{H} - 7 \left(\frac{T}{H} \right)^{0.222} \right) \cdot \left(\frac{H}{S} \right)^{1.34} \tag{4.7}$$

where ε_{ox} and ε_0 are the silicon oxide and the vacuum permittivity, S the inter-line gap. An average value of the width W in the formulae (from equation(4.4) to equation(4.7)) is used as signal and ground lines are geometrically different in width.

For the calculation of the medium-density TSV compact model resistance and oxide capacitance, we propose our own analytical expressions. Since the TSV is a conic structure, the expressions are derived from the formulae defining a perfect cylindrical conductor on which we have applied, along the conductor length, linear variations for the thickness and radius.

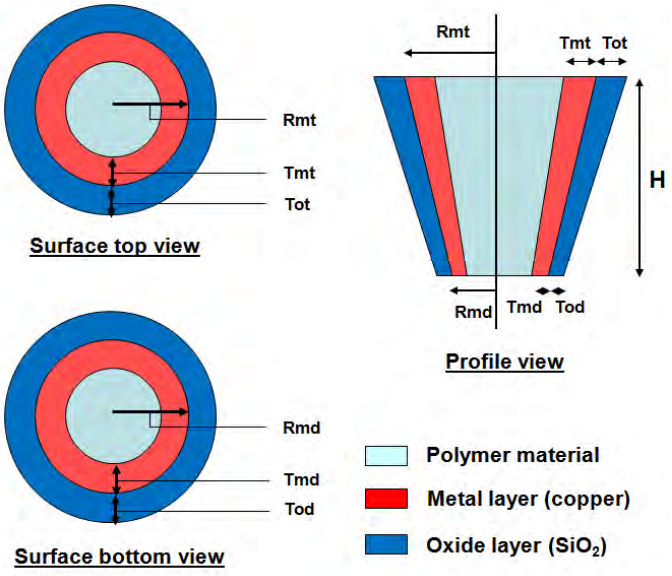


Figure 4-3 Medium-TSV schematic.

$$Rot = Rmt + Tot \tag{4.8}$$

$$Rod = Rmd + Tod \tag{4.9}$$

$$R_{TSV} = \frac{H}{\pi\sigma}\frac{1}{2\left(Rmt\cdot Tmd - Rmd\cdot Tmt\right)}\ln\left(\frac{Tmd}{2Rmd - Tmd}\cdot\frac{2Rmt - Tmt}{Tmt}\right) \tag{4.10}$$

$$C_{ox(TSV)} = \frac{\varepsilon_0\varepsilon_{ox}\cdot 2\pi\cdot H}{Tot - Tod}\left[Rot - Rod + \frac{Rot\cdot Tod - Rod\cdot Tot}{Tot - Tod}\ln\left(\frac{Tod}{Tot}\right)\right] \tag{4.11}$$

where:

Rmt and *Tmt* are the copper layer radius and thickness of the TSV top surface, respectively;

Rot and *Tot* the oxide layer radius and thickness of the TSV top surface;

Rmd and *Tmd* the copper layer radius and thickness of the TSV bottom surface;

Rod and *Tod* the oxide layer radius and thickness of the TSV bottom surface.

All the radii and thicknesses are indicated on the TSV schematic shown on Figure 4-3. As an example, when the TSV is in W1 configuration (see next section), these geometries are equal to: *Rmt* = 30 µm, *Rmd* = 29.5 µm, *Tmt* = 1 µm, *Tmd* = 3µm, *Tot* = 0.2 µm, *Tod* = 0.5 µm.

The polymer material filling the TSV does not significantly affect its RF behaviour. Additionally, the variations of the TSV radius and the copper layer thickness are very low. Consequently, the analytical expressions of a filled cylindrical conductor are still used in order to calculate the self and mutual inductances.

$$L_{TSV} = \mu_0\mu_r\frac{H}{2\pi}\left[\sinh^{-1}\left(\frac{H}{R_a}\right) + \frac{R_a}{H} + 0.15 + \sqrt{\left(\frac{R_a}{H}\right)^2 + 1}\right] \tag{4.12}$$

$$M_{TSV} = \mu_0\mu_r\frac{H}{2\pi}\left[\sinh^{-1}\left(\frac{H}{p}\right) + \frac{p}{H} - \sqrt{\left(\frac{p}{H}\right)^2 + 1}\right] \tag{4.13}$$

where p is the pitch between two nearby TSVs and R_a the TSV average radius.

4.2.2 Global electrical context modeling

The modelling of the global electrical context will be illustrated in this part for the cases of the coplanar waveguides and TSV chains. Since the substrate is highly conductive for the investigated coplanar waveguides, it can be modelled as a very low resistance or a simple node. For each coplanar line, the vertical current path in the epitaxial layer is modelled by a resistance (R_{epi}) in parallel with a capacitance (C_{epi}). The environment modelling also contains the oxide layer capacitances (C_{ox}) isolating the lines from the substrate.

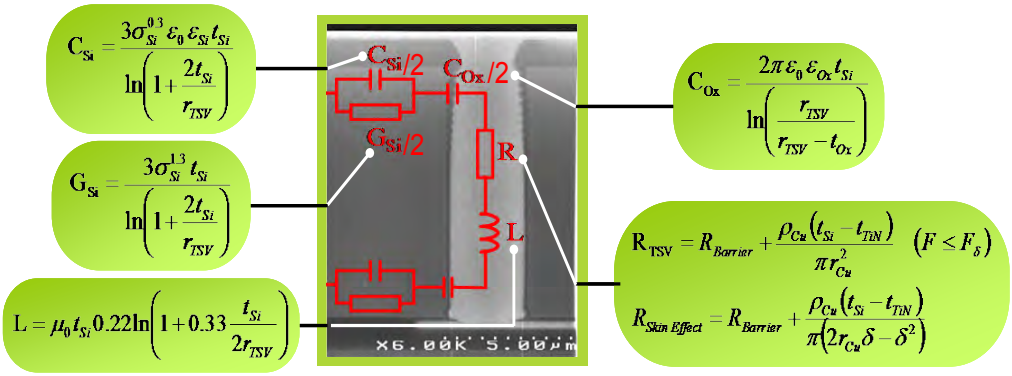


Figure 4-4 Analytical model for High Density TSV ([129])

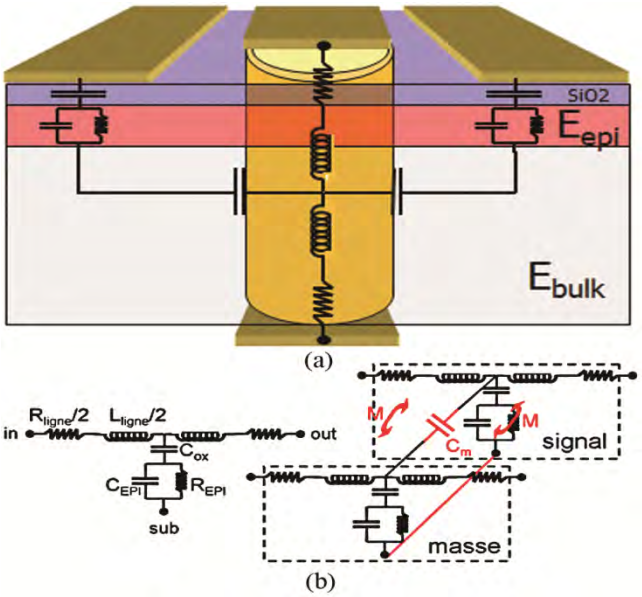


Figure 4-5 (a) Medium-density TSV front views and compact modeling of the medium-density TSV including the current path (b)'RLCG' compact modeling of the signal line and one ground line of the coplanar waveguide.

$$R_{epi} = \rho_{epi}\frac{T_{epi}}{W \cdot L} \tag{4.14}$$

$$C_{epi} = \frac{\varepsilon_0\varepsilon_{epi} \cdot L \cdot W}{T_{epi}} \tag{4.15}$$

$$C_{ox} = \frac{\varepsilon_0\varepsilon_{ox} \cdot L \cdot W}{T_{ox}} \tag{4.16}$$

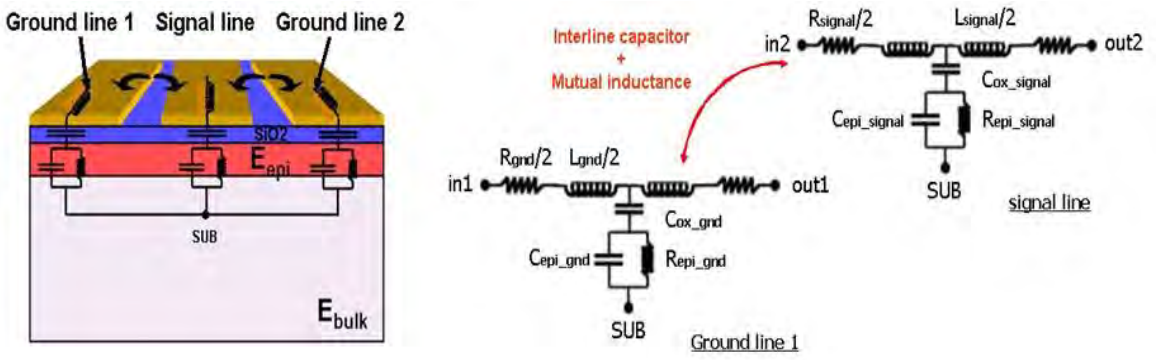


Figure 4-6 Left: Coplanar waveguide front view. Right: RLCG compact modeling of the signal line and one ground line of the coplanar waveguide

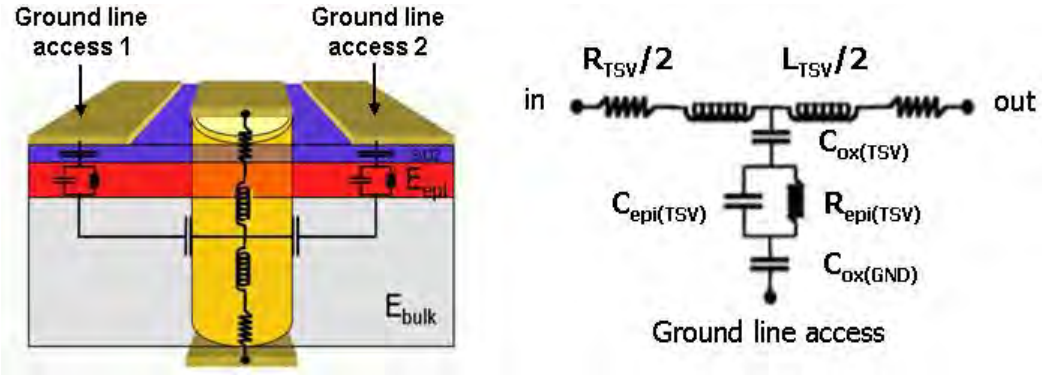


Figure 4-7 Left: Medium-density TSV front view. Right: RLCG compact modeling of the medium-density TSV including the current path.

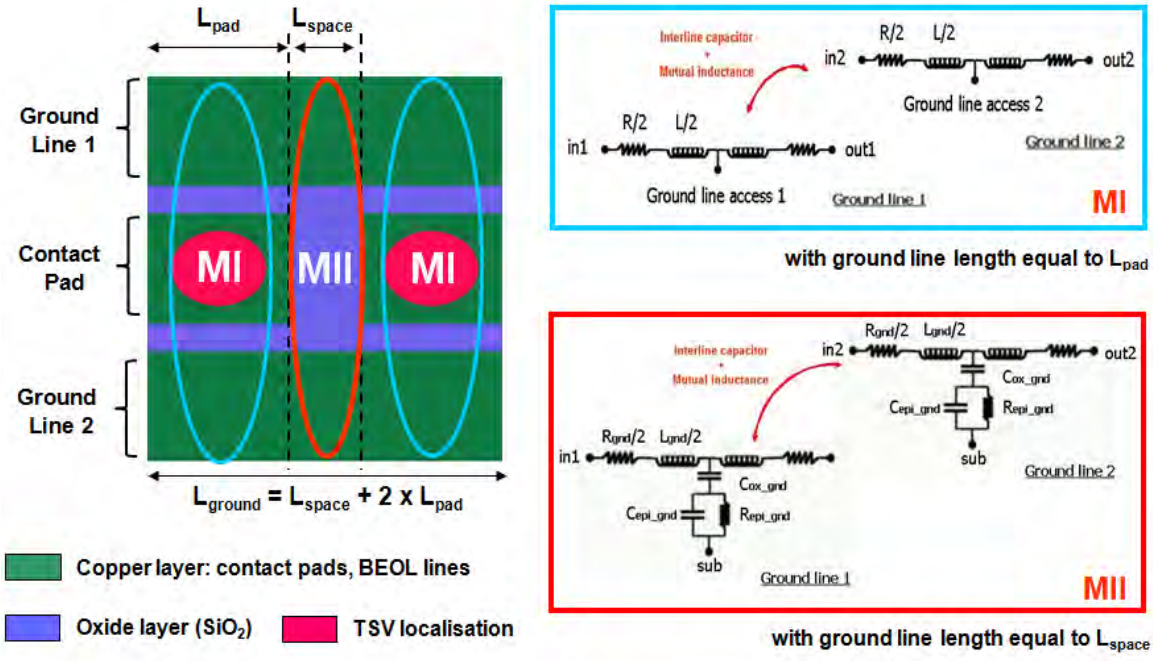


Figure 4-8 Decomposition, for the 2xTSV chain, of the BEOL ground lines into RLCG serial blocks depending on the considered surface (MI and MII models).

The electrical parameter values must be adapted if the compact model is to depict a lumped model or an elementary cell of a distributed model. The coplanar waveguide model is illustrated in Figure 4-6 with all the lines connected to the substrate through a node SUB. Depending on the system geometrical and technological data, the inductive coupling between the two ground lines can be neglected or not.

In the TSV chain, the currents are flowing vertically through the epitaxial and the oxide layers to reach the ground planes corresponding to the BEOL level ground lines (Figure 4-7). The electrical parameters of the epitaxial and oxide layers ($R_{epi(TSV)}$, $C_{epi(TSV)}$ and $C_{ox(GND)}$) are calculated in the same way as the coplanar waveguide using expressions (equation (4.14) to equation (4.16)). As an approximation in the investigated frequency domain, the couplings existing between the substrate and the TSVs (TSV/substrate couplings) are not considered. Only the proximity effects between TSVs (TSV/TSV couplings) have been taken into account. The TSV chain electrical context modelling involves dividing the BEOL ground lines into serial blocks, by dissociating the parts reached on the overall surface by the current coming from the TSVs. These surface parts have a length corresponding to that of the TSVs contact pads L_{pad}. The width and the thickness remain unchanged for the entire line surface. Hence the epitaxial layer parameters ($R_{epi(TSV)}$, $C_{epi(TSV)}$), as well as the oxide capacitance ($C_{ox(GND)}$), modelling the current path going through the TSV to the ground line, must be calculated for $L = L_{pad}$.

The parts of the surfaces of the ground lines involved in the current paths are simply modelled by RL networks; otherwise they are modelled as shown in Figure 4-6. As an illustration, the Figure 4-8 shows how the two ground lines are decomposed into serial blocks in the case of a chain of two TSVs (2xTSV chain). The parts of the lines concerned in the current pathway are modelled as MI; the remaining surfaces as MII. The total wire length, L_{ground}, is equal to twice the contact pad length, L_{pad}, plus the BRDL line length, L_{space}, also corresponding to the gap between the two contact pads. Like the BEOL ground lines, the BRDL line connecting the two TSVs is described by an oxide capacitance reaching the substrate single node (Figure 4-9) where there are also connected the BEOL ground line surfaces corresponding to the contact pads gap (MII).

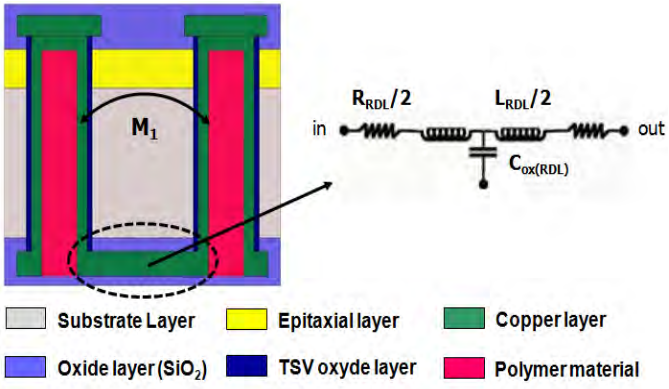


Figure 4-9 2xTSVs chain side view. Left: representation of the inductive coupling between the TSVs. Right: RLCG compact model of the BRDL line.

From the way the TSVs are connected, the 2xTSV chain can be seen as a “U-shaped” structure. For nxTSV chains, n/2 “U-shaped” structures are connected at the BEOL level by contact pads and a 60 µm length access line, whatever the configuration. Figure 4-10 shows the profile view of a 4xTSV chain; proximity effects between the TSVs are also represented. The BEOL ground line total length thus equals:

$$L_{BEOL} = nL_{pads} + \frac{n}{2}L_{space} + \left(\frac{n}{2} - 1\right)L_{access} \tag{4.17}$$

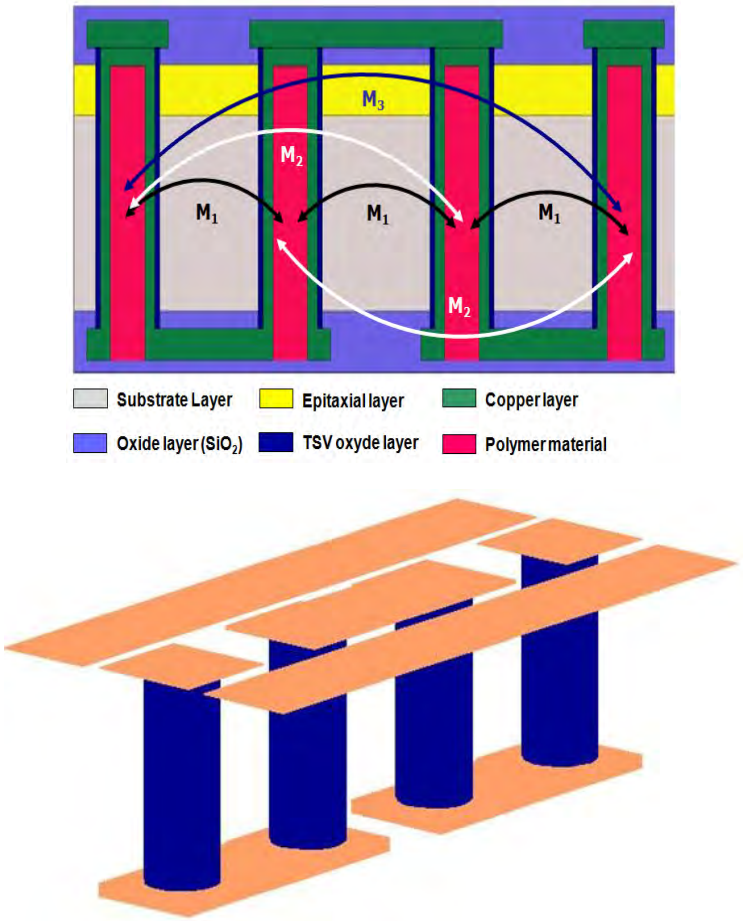


Figure 4-10 4xTSV chain side view: representation of the proximity effects between TSVs (inductive couplings). The two chains of 2xTSV are connected at the BEOL level with contact pads and an access interconnection line.

Figure 4-11 illustrates the ground lines decomposition into serials blocks in the case of the 4xTSV chain. The decomposition can be extended for chains including a higher number of TSVs. The contacts pads and the access line connecting the inner TSVs are modelled as a single transmission line, depicting then a coplanar waveguide regarding the concerned ground lines surfaces.

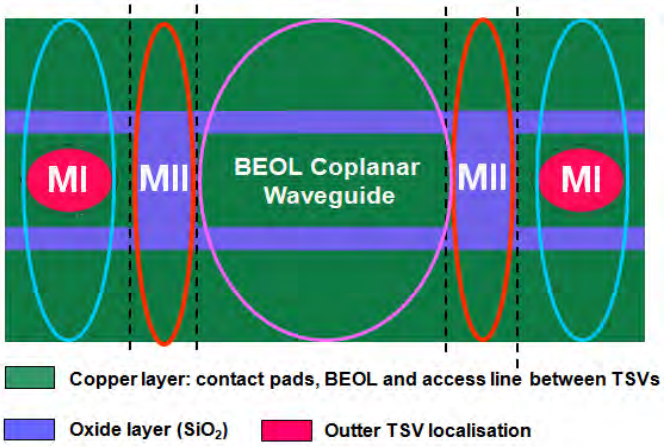


Figure 4-11 4xTSV chain top view: decomposition of the BEOL ground lines into serial blocks. Depending on the surface concerned, lines are modeled as a coplanar waveguide, MI or MII.

4.3 3D Transmission Line Extractor 3D-TLE

4.3.1 Substrate modeling approach

The modeling of a conductive substrate as a simple node is only viable for low and medium frequency domains. At high frequency, the substrate coupling effects must be added to the system electrical modeling by representing the substrate as a RLCG network to more accurately evaluate the IC's losses. The modeling can become rapidly complex since the coupling effects must be considered between of all the components of the chip. Moreover, the substrate can be non-uniform with different doping values, i.e. having different resistivity and permittivity throughout the considered volume. The substrate is therefore modeled as a stack of parallel heterogeneous dielectric layers because the doping profile evolves in the perpendicular direction to the Si-SiO2 surface [130].

As a consequence, the extraction method in last chapter is applied here. Generally, a current is applied on a contact pad which can be located atop or inside the substrate. A voltage is then measured at the level of another contact, enabling one to deduce a square transfer impedance matrix [Z_T] it was shown that it was shown that whose dimensions correspond to the number of contacts. The substrate coupling between two elements is generally modeled by a resistance in parallel with a capacitance. To extract the values of the overall resistances and capacitances constituting the substrate network from the elements of Z_T, the matrix is inverted to obtain a conductance matrix G_T and a nodal analysis using Kirchhoff's Current Law (KCL) is applied.

The method can be used for high resistive and high conductive substrates which may or may not be uniform. Moreover, the values of the substrate network electrical parameters can be given at DC or evolving with the frequency. A more detailed description of the method can be found in Chapter 3 and our articles [131] and [132].

The method in this chapter is applied in the example of a 240 µm line length coplanar waveguide atop a high resistive substrate without an epitaxial layer. The coplanar lines can be assimilated to three contacts. The material and technological data considered for the metal and oxide layers are the same as those in the CPW test structure in its W1 configuration. The substrate height is equal to 120 µm, its permittivity to 11.7 and its resistivity is fixed to 60 Ω•cm. Figure 3-1 illustrates the corresponding substrate compact model.

4.3.2 3D Transmission Line Extractor 3D-TLE

Because systems descriptions can become complex when considering the global electrical context and the compact models' distribution, we developed using Matlab® [133] a 3D extraction tool, 3D-TLE (3D Transmission Line Extractor), based on our modelling approach and which integrates the substrate extraction method algorithm (Figure 4-12). Through a hierarchical syntax and specific statements, one depicts in a text file the geometrical and technological data of the system by defining: its layers; the type of components comprised in the system; the connectivity between chip elements, which are instantiated components; and the element interactions (couplings, interactions with layers for current path modelling).

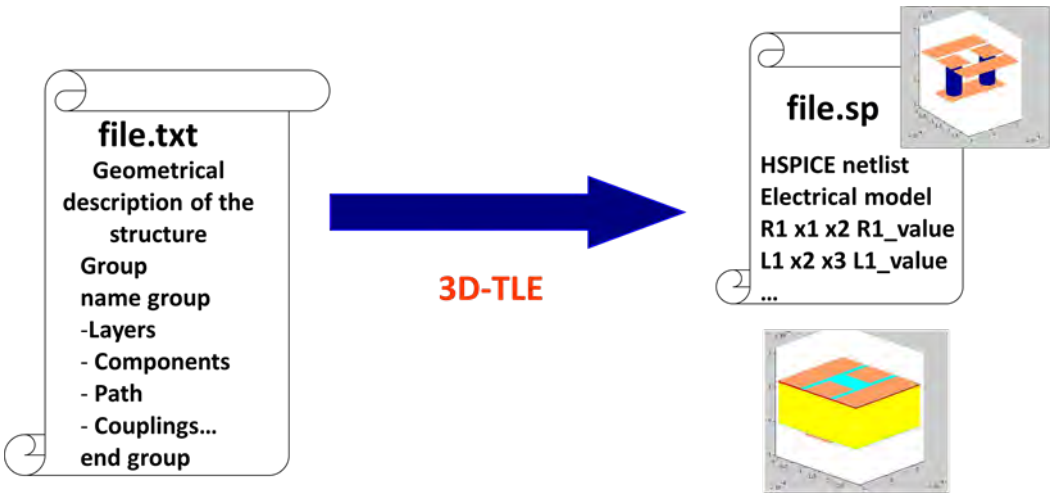


Figure 4-12 Environment of 3D extraction tool 3D-TLE.

The extraction tool generates from this text file a SPICE netlist, containing the system RLCG electrical description, exportable toward CAD tools such as Agilent Technologies ADS® [134]. The viability of 3D-TLE was checked through S-parameter comparisons for given systems between their 3D-TLE SPICE netlists and their schematics designed under ADS®. As the expected results show that the responses are the same; however describing the structure using 3D-TLE is easier and faster than designing it manually using the CAD tool. 3D-TLE provides also the system 3D picture.

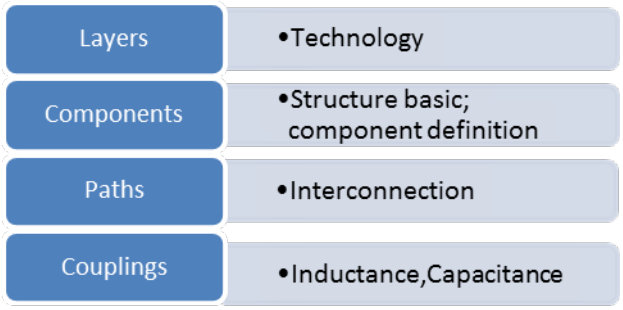


Figure 4-13 File structure of the text file to define a specific substrate structure.

An example of a structure description used to 3D-TLE and the generated SPICE netlist is shown in the following Table 4-1.

Table 4-1 An example of a structure description used to 3D-TLE and SPICE netlist generated

Input file for 3D-TLE **(description of the structure)**	**Netlist** **The nodes input and output are:** **in, out, mass_in, mass_out**
*Model 3DIDEAS GROUP 3DIDEAS_config2 #LAYERS SUB 1 0 0 0 W=270E-6 L=380E-5 T=725E-6 rho=1E-2 epsr=11.7 OXI 1 0 0 725E-6 W=270E-6 L=380E-5 T=0.9E-6 epsr=5.2 BEOL 1 T=6.7E-6 rho=2.2e-8 #COMPONENTS LINE 1 BEOL 1 W=70E-6 L=380E-5 inter OXI(1)->subnode(1) #PATHS LINE 1 gnd1 0 0 725.9E-6 mass_in mass_out coupled LINE 1 signal 100E-6 0 725.9E-6 in out coupled LINE 1 gnd2 200E-6 0 725.9E-6 mass_in mass_out coupled #COUPLINGS LINE gnd1 LINE signal LINE gnd2 end group end	*Netlist generated from 3DIDEAS_config2 .subckt gnd1_signal_gnd2 in1 out1 in2 out2 in3 out3 sub_x1 R1 in1 x1_gnd1 0.089126 L1 x1_gnd1 x2_gnd1 1.9372e-09 L2 x2_gnd1 x3_gnd1 1.9372e-09 R2 x3_gnd1 out1 0.089126 Cox_gnd1 x2_gnd1 sub_x1 1.3601e-11 R3 in2 x1_signal 0.089126 L3 x1_signal x2_signal 1.9372e-09 L4 x2_signal x3_signal 1.9372e-09 R4 x3_signal out2 0.089126 Cox_signal x2_signal sub_x1 1.3601e-11 R5 in3 x1_gnd2 0.089126 L5 x1_gnd2 x2_gnd2 1.9372e-09 L6 x2_gnd2 x3_gnd2 1.9372e-09 R6 x3_gnd2 out3 0.089126 Cox_gnd2 x2_gnd2 sub_x1 1.3601e-11 K1 L1 L3 0.65818 K2 L2 L4 0.65818 Cinter1 x2_signal x2_gnd1 5.4228e-14 K3 L3 L5 0.65818 K4 L4 L6 0.65818 Cinter2 x2_gnd2 x2_signal 5.4228e-14 K5 L1 L5 0.52744 K6 L2 L6 0.52744 .ends gnd1_signal_gnd2 X1_gnd1_signal_gnd2 **mass_in mass_out in out mass_in mass_out** 0 gnd1_signal_gnd2 .end

When getting the SPICE netlist file from 3D-TLE, one can import it to the ADS easily. A screenshot of the simulation in the ADS with structure described by 3D-TLE is shown in the following Figure 4-14.

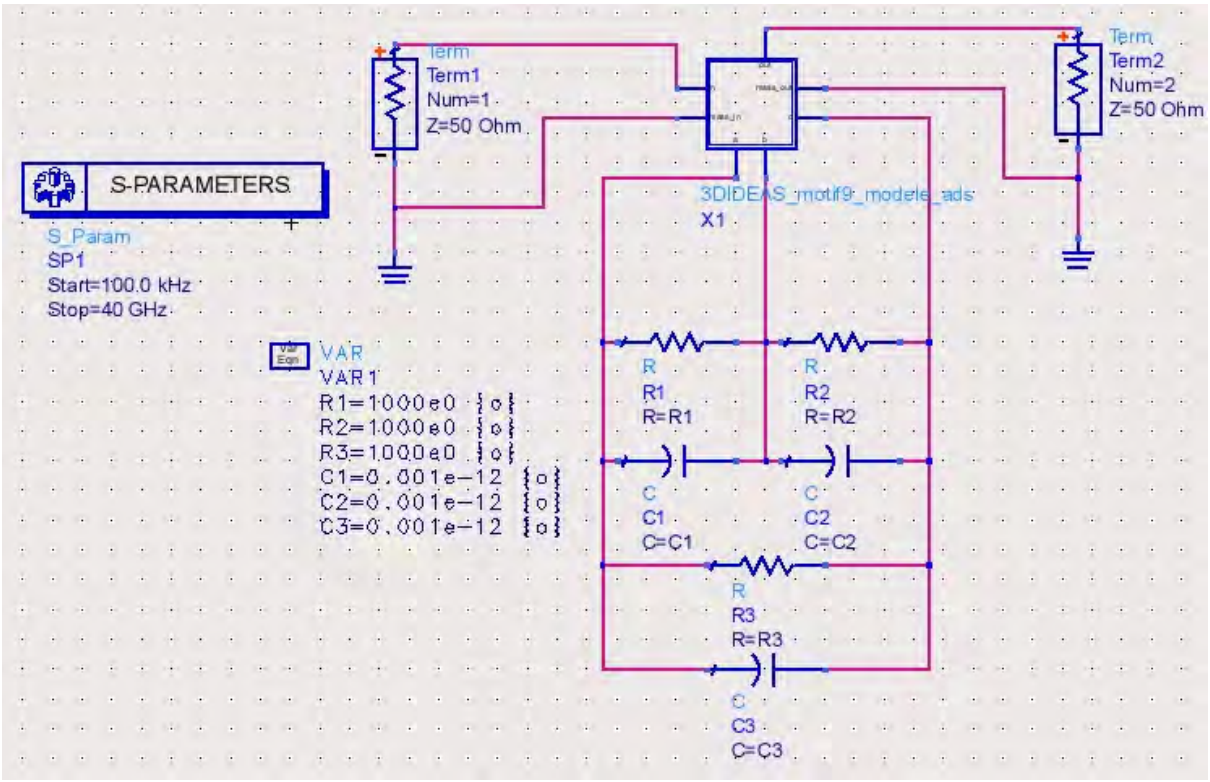


Figure 4-14 Screenshot of the simulation in the ADS with structure described by 3D-TLE

Without the use of 3D-TLE, the designing of structure manually using the CAD tool becomes more complicated maybe as shown in following Figure 4-15.

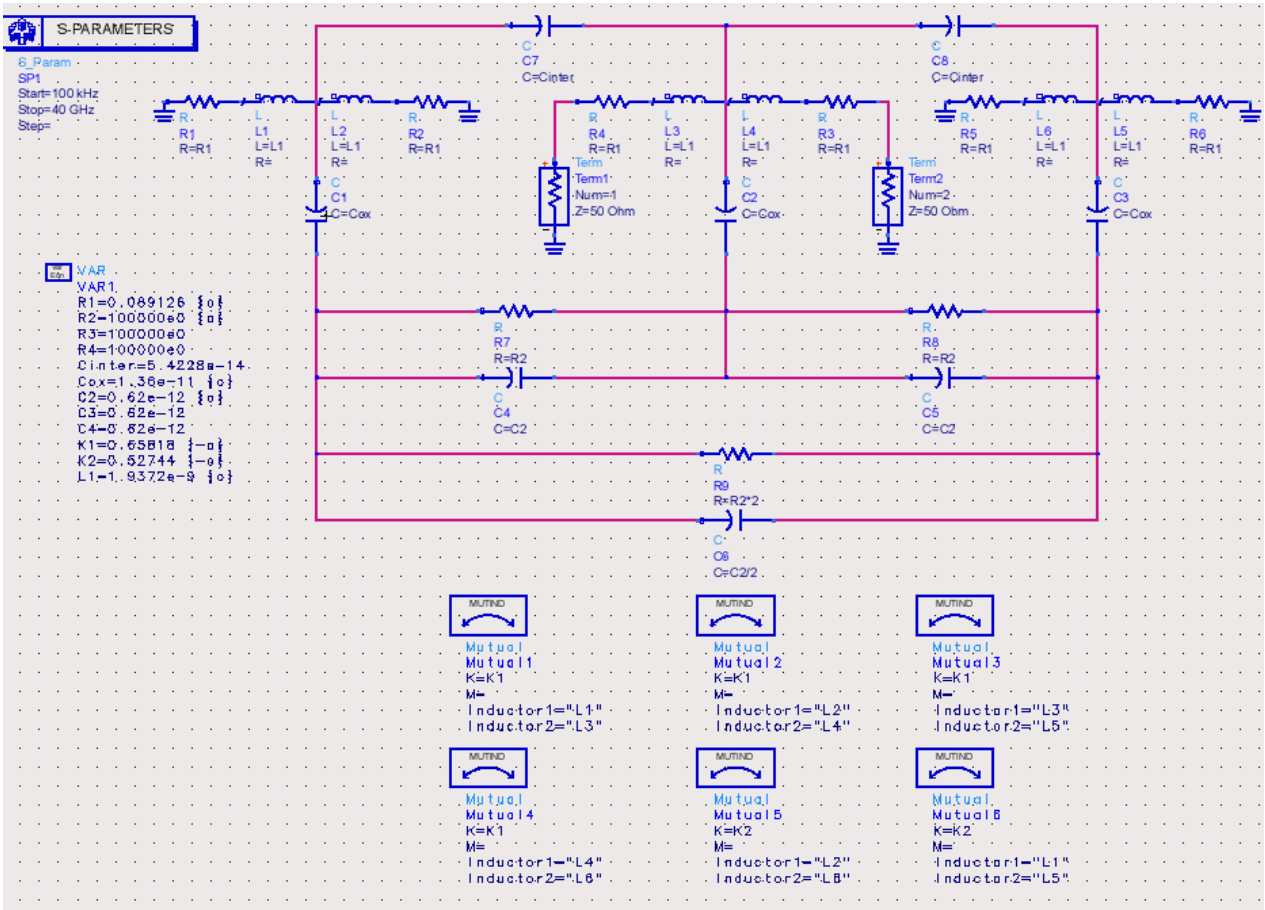


Figure 4-15 Screenshot of the simulation in the ADS without use of netlist from 3D-TLE

4.4 Modeling Approach Validation and Test Structures' RF Behaviors

In this section, the modeling approach is validated in the frequency domain via S-parameter comparisons between the measurements performed on the test structures, for two different configurations, and the simulation results from their equivalent electrical models. The test structures used will be presented at first, and then the comparison between the test and the simulation will be given.

4.4.1 Presentation of test structures used

At first, a simple structure for coplanar waveguide (CPW) is tested as shown in following Figure 4-16.

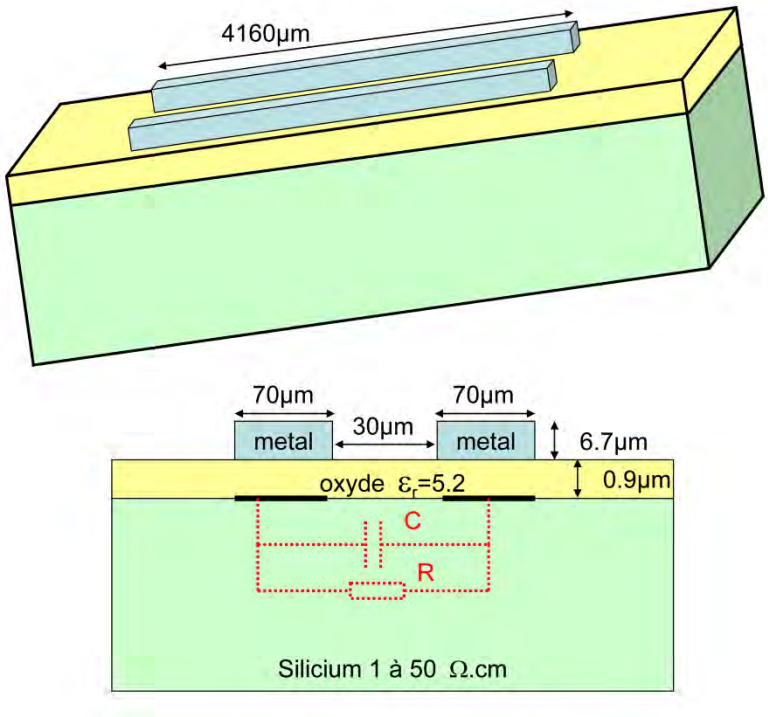


Figure 4-16 Schematic of a CPW structure used to test (Source: LETI)

Then two more complicated substrate structures are applied for the modeling approach. The first one is the Back-End-Of-Line (BEOL) CPW, which is used as a redistribution metal line to propagate electrical signals along the top or the backside of the stacked dies. The second one, which we will denote hereafter as TSV chain or nx TSV chain, consists in *n* medium-density TSVs connected at the backside of the chip with a Back RDL (BRDL) redistribution line. The TSVs are connected to the BEOL level, where the ground lines are located, by means of square contact pads. The physical views of a coplanar waveguide and a chain of 2 TSVs (2xTSV chain) are represented in Figure 4-17.

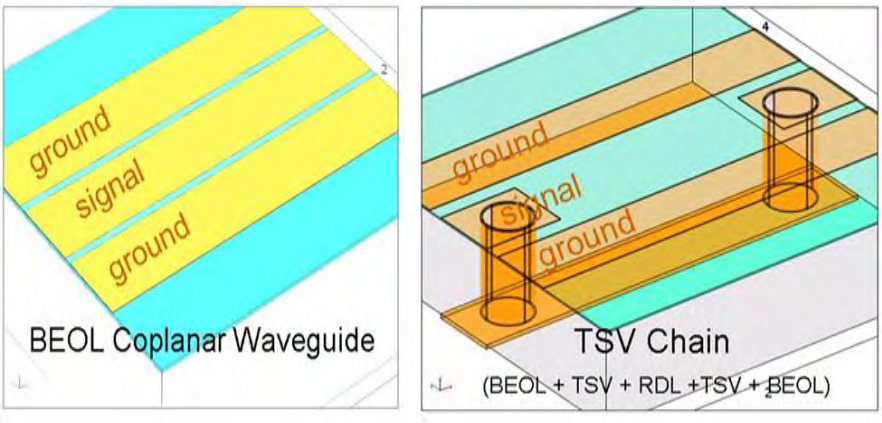


Figure 4-17 Physical views of some test structures. Left: a BEOL coplanar waveguide. Right: a chain of 2 TSVs (2xTSV chain).

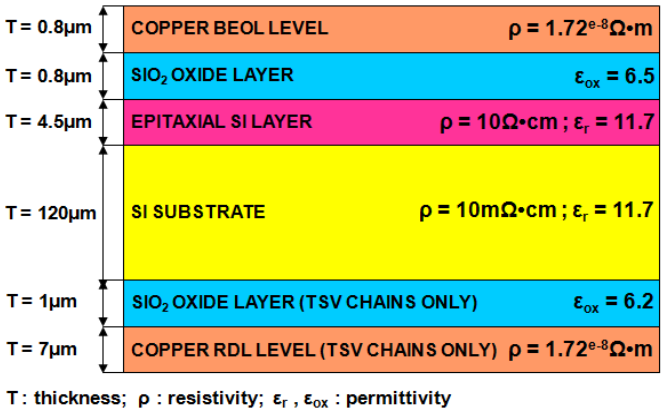


Figure 4-18 Geometrical and technological data of the layers comprised in the CPW and TSV chain structures.

The test structures are realized using a highly conductive silicon substrate having a thickness of 120 µm, a resistivity ρ=10 mΩ•cm, and a permittivity ε_r =11.7. On the substrate is deposited a thin epitaxial layer (thickness: 4.5 µm, resistivity: 10 Ω•cm, permittivity: 11.7). The lines at the BEOL level, for CPWs and TSV chains, are isolated from the substrate by an oxide layer (thickness: 0.8 µm, permittivity: 6.2). Regarding the TSV chains, an oxide layer (thickness: 1 µm, permittivity: 6.5) is added at the backside of the structures to isolate the BRDL line from the substrate. All the layers used for the CPW and the TSV chain structures are represented in Figure 4-18 with their respective characteristics. For the BEOL level line chunks have a thickness of 0.8 µm, whereas they are 7 µm for the RDL level.

The CPW structures are made with three copper lines. Two configurations, called W1 and W2, are considered for these structures. For the W1 configuration, the width of the signal line is equal to 90 µm (60 µm for W2) with spacing between lines of 15 µm (30 µm for W2); the width of the ground lines equals 80µm whatever the configuration. Three different coplanar line lengths have been investigated for W1 and W2 configurations; the values are: 60 µm, 240 µm and 540 µm. A top view of the CPW is presented in Figure 4-19 with all the geometrical data indicated with the exception of the thickness.

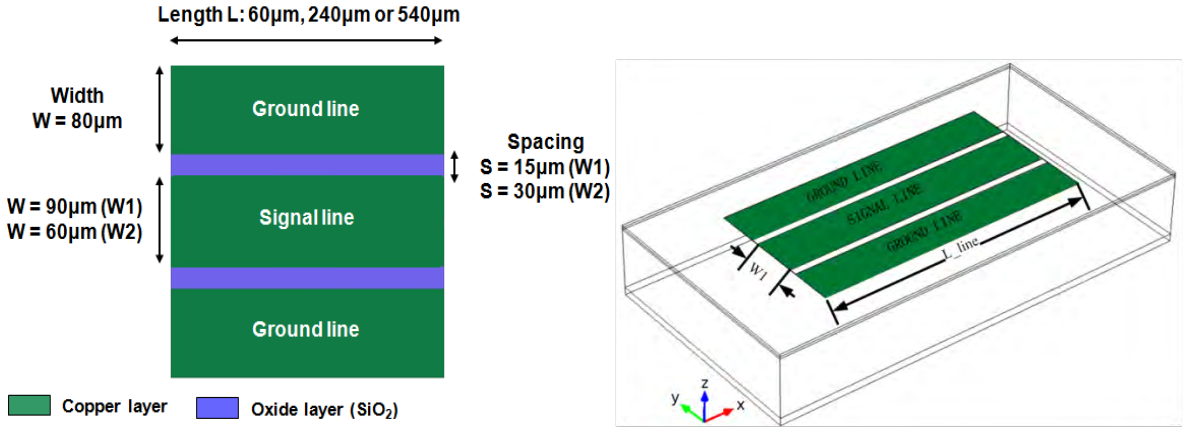


Figure 4-19 Top view (left) and 3D view (right) of a CPW structure.

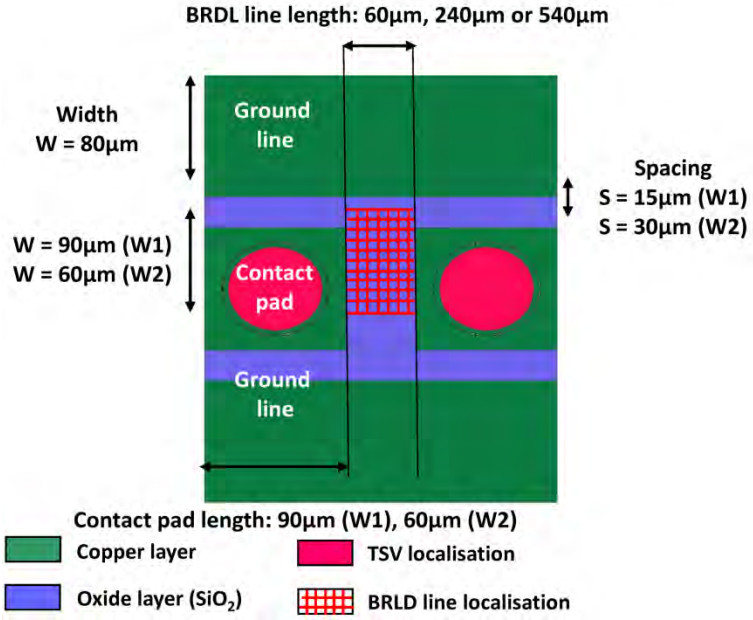


Figure 4-20 Top view of a 2xTSV chain structure configuration

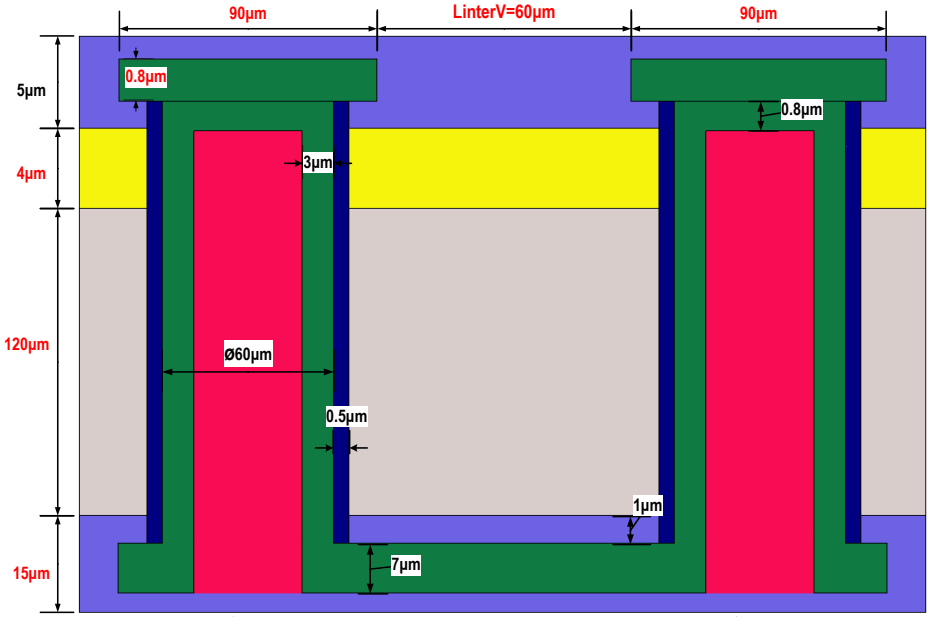


Figure 4-21 Cross-section view of a 2xTSV chain structure configuration

For the TSV chains, the BRDL line length can have one of three values: 60 µm, 240 µm and 540 µm. As with the CPWs, there are two configurations for the TSV chain. In the W1 configuration, the width of the BRDL line and the contact pads is 90 µm (60 µm for W2). The distance separating the contact pads and the ground lines also depends on the configuration. The values of the spacing are identical to those for the CPW structures; as are the ground line widths. Figure 4-20 shows the top view of the 2xTSV chain and Figure 4-21 shows the cross-section view. For sake of clarity, the BRDL line and the contact pads localizations are indicated on them.

The different colors represent different materials.

Table 4-2 Domain physics properties

Color	*Material*	*Physics property*	*Description*
	Copper	σ=5e7S/m	M1 and the TSV
	SiO_2	ε_r=6.6	Top Oxide layer and back Oxide layer
	SiO_2	ε_r=6.5	Surface of TSV called sidewall SiO2
	Si Epitaxial	σ=10S/m ε_r=11.7	Epitaxial layer
	Silicon	σ=10^4S/m ε_r=11.7	Silicon bulk
	SINR	ε_r=3.4	Filling TSV

Finally, the medium-density TSV used is a large copper tubular conic structure, isolated from the silicon substrate with silicon oxide (ε_{ox}=6.5) on the TSV walls and filled with polymer material. The SEM cross section of such a TSV is observable in Figure 4-22. One can note from this figure that the TSV diameter increases towards the TSV top surface at the BEOL level, whereas the thicknesses of the copper and oxide layers decrease. For the TSV chain W1 configuration, the TSV diameter, including the copper layer and the polymer material, varies from 60 µm to 59 µm (from 40µm to 37µm for W2). For configurations, The TSV copper and SiO_2 layers thicknesses vary at each extremity from 1µm to 3µm and from 0.2µm to 0.5µm, respectively (Table 4-3). All the TSV fabrication process details are reported in [135].

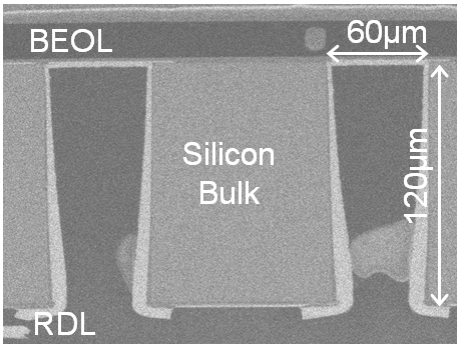


Figure 4-22 SEM cross section of the medium-density TSV used in the TSV chains (W1 configuration).

Table 4-3 SEM cross section of the medium-density TSV used in the TSV chains (W1 and W2 configurations)

TSV geometrical variations	BEOL LEVEL	RDL level
TSV diameter (polymer material + copper layer)	60µm (W1) 40µm (W2)	59µm (W1) 37µm (W2)
TSV copper layer thickness	1µm	3µm
TSV oxide layer thickness	0.2µm	0.5µm

4.4.2 Experiment test method and technology

In the electrical field of the microwave, the characterization of interconnect is defined as an equivalent electric model extracting from its measures. For example, it is extracted as a function of frequency, the characteristic impedance and propagation exponent or distributed elements R, L, C and G of the equivalent model from the telegraph equation and that from measurement of the scattering matrix [S] of this interconnection on a wide range of frequency using a vector network analyzer (VNA). In practice, this interconnection that can be called Device Under Test (DUT), is generally in a complex test environment does not allow the experimenter to extract its parameters by a single measurement. In fact, this interconnection is buried in a cell to connect to the measurement system (in the general case we find the presence of contact pads, sections of access, cables, connection lines ....). "De-embedding" methods is used to avoid the influence of the environment and then get the intrinsic characteristics of the DUT, for us the interconnection, from those of the cell.

The modeling approach then relies on analyzing the test structures by means of a 3D full-wave electromagnetic tool using the Finite Element Method (FEM)[104] to understand the physical and electrical phenomena occurring in 3D interconnects during signal propagation; and finally on the use of the Transmission Line Method.

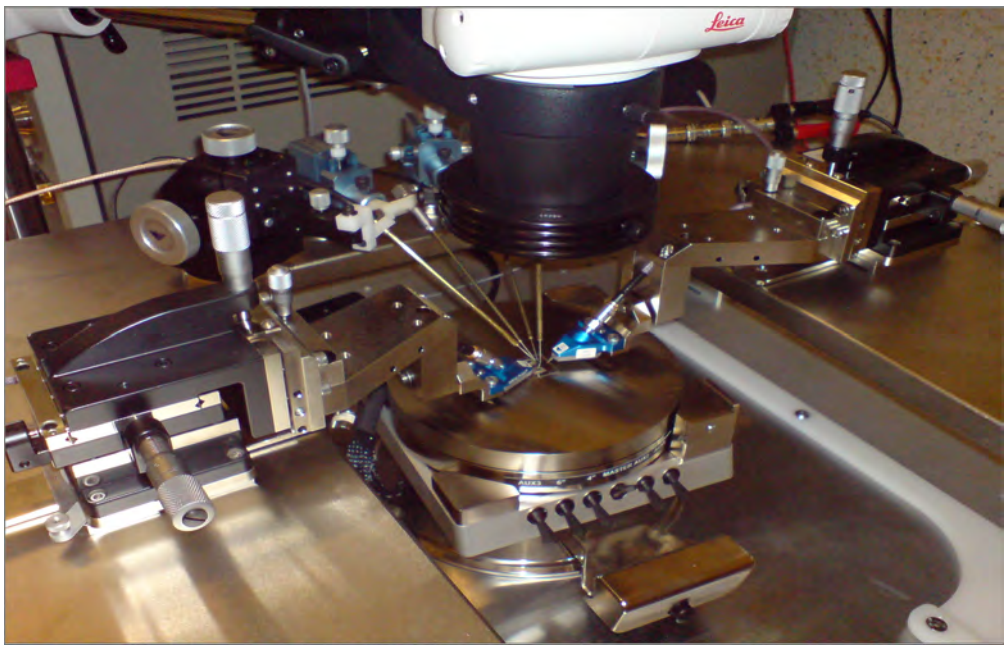
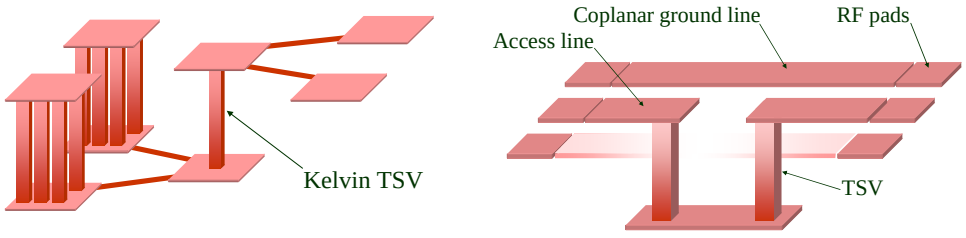


Figure 4-23 Measurements with a Vector Network Analyzer (VNA) for a frequency sweep

To characterize accurately the resistance of single TSV, Kelvin structures are designed and processed. An array of twenty-five 3 µm wide and 5 µm-space TSV connects 80x80 µm² copper pads to top metal level as shown in Figure 4-24 (a). Besides, specific RF structures were integrated to evaluate TSV behavior with frequency. These coplanar structures include Ground Signal Ground pads, access lines and dual via chains. Figure 4-24 (b) shows a schematic view of the RF devices.



(a) (b)

Figure 4-24 Schematic view of Kelvin TSV (a) and microwave structures (b)

RF structures are tested with a Vector Network Analyzer (VNA) and 100 µm pitch Ground-Signal-Ground (GSG) probes. The VNA provides frequency sweep typically from 20 MHz up to 70 GHz, and measures transmitted and reflected waves to build scattering matrix [S]. Both calibration and de-embedding operations enable to adjust reference planes to accurately measure the properties of TSVs.

It is essential to specify, through a measure microwave, a first procedure for calibrating the device, before the vector network analyzer is performed. The Thru-Reflect-Line (TRL) de-embedding technique is applied to remove from the S-parameters measurements the contact and access lines effects, and thus obtain the test structures' actual RF behaviors[136] which removes parasitic effects from wires and probes. [137-140]

It consists in measuring four standard devices (SOLT) to refer the tip of the probe at standard 50Ω impedance by subtracting parasitic elements of cable and probes. Then, a de-embedding step is required to remove pad and access line and adjust reference planes as close as possible to the TSV in order to extract intrinsic TSV [S] matrix. This de-embedding is performed by computation and lead to determine intrinsic TSV S-parameters. The first step consists in calculating the so-called [ABCD] chain matrices from [S] matrices, best suited to manipulate. Then [ABCD] matrices of RF pad, access line and full structure, respectively named $[A]_{pad}$, $[A]_{line}$ and $[A]_{device}$, are extracted from de-embedding measurements. Finally, TSV matrix is built, removing RF pad and access line effects:

$$[A_{TSV}] = [A_{line}]^{-1} \times [A_{pad}]^{-1} \times [A_{device}] \times [A_{pad}]^{-1} \times [A_{line}]^{-1} \qquad (4.18)$$

A last calculation step allows to switch from [ABCD] to the TSV chain [S] matrix.

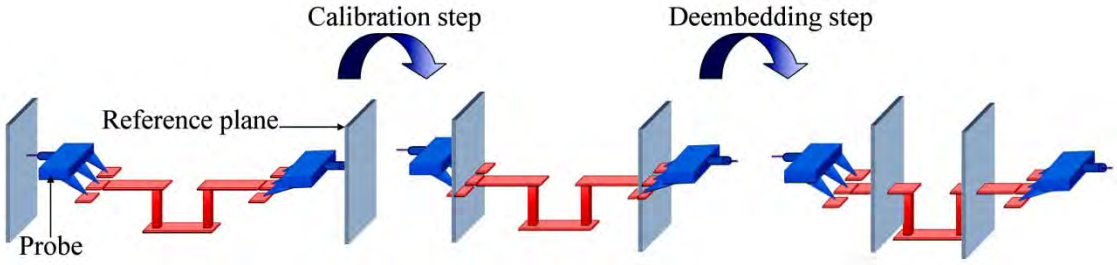


Figure 4-25 Calibration & de-embedding effect

4.4.3 Finite Element Method simulation

4.4.3.1 Module introduction

The simulation is based on the Radio Frequency module. One major difference between quasi-static and high-frequency modeling is that the formulations depend on the electrical size of the structure. This dimensionless measure is the ratio between the largest distances between two points in the structure divided by the wavelength of the electromagnetic fields. For simulations of structures with an electrical size in the range up to 1/10, quasi-static formulations are suitable.[141] The physical assumption of these situations is that wave propagation delays are small enough to be neglected. Thus, phase shifts or phase gradients in fields are caused by materials and/or conductor arrangements being inductive or capacitive rather than being caused by propagation delays. For electrostatic, magnetostatic, and quasi-static electromagnetics, use the AC/DC Module, a COMSOL Multiphysics add-on module for low-frequency electromagnetics. When propagation delays become important, it is necessary to use the Maxwell equations ($curl\vec{E}, curl\vec{H}$) for very high-frequency electromagnetic waves. They are appropriate for structures of electrical size 1/100 and larger. Thus, an overlapping range exists where we can use both the quasi-static and the full Maxwell physics (this latter one being solved in time domain; not exist in CMOSOL).

4.4.3.2 Domain setting

The “W1 Lines” is similar to the “W1 Via” but without “TSV” or “RDL”. The “whole model” is shown as following,

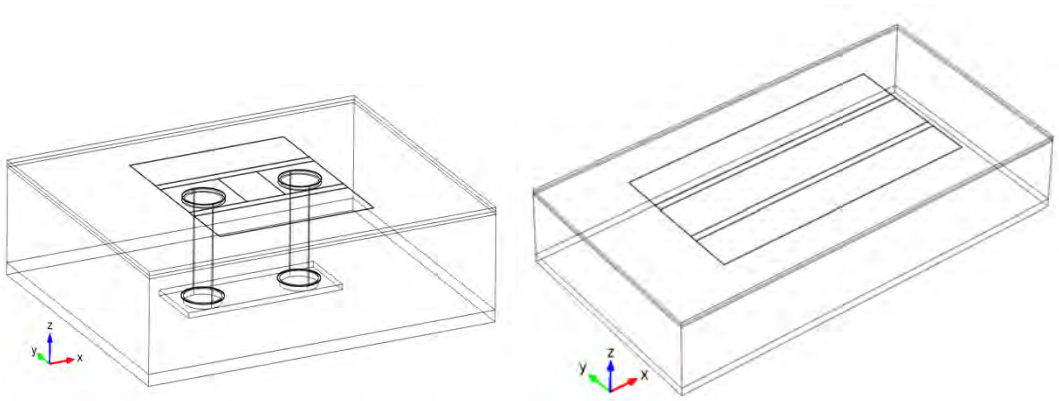


Figure 4-26 whole model for 2TSV and CPW

Basis on the symmetric property of the model, we can just simulate half of it in the COMSOL in order to save the simulation time and the memory consumption.

To improve the accuracy to have good boundary condition, we add two air areas on and under the model. The finally “half-model” is shown in following Figure 4-27.

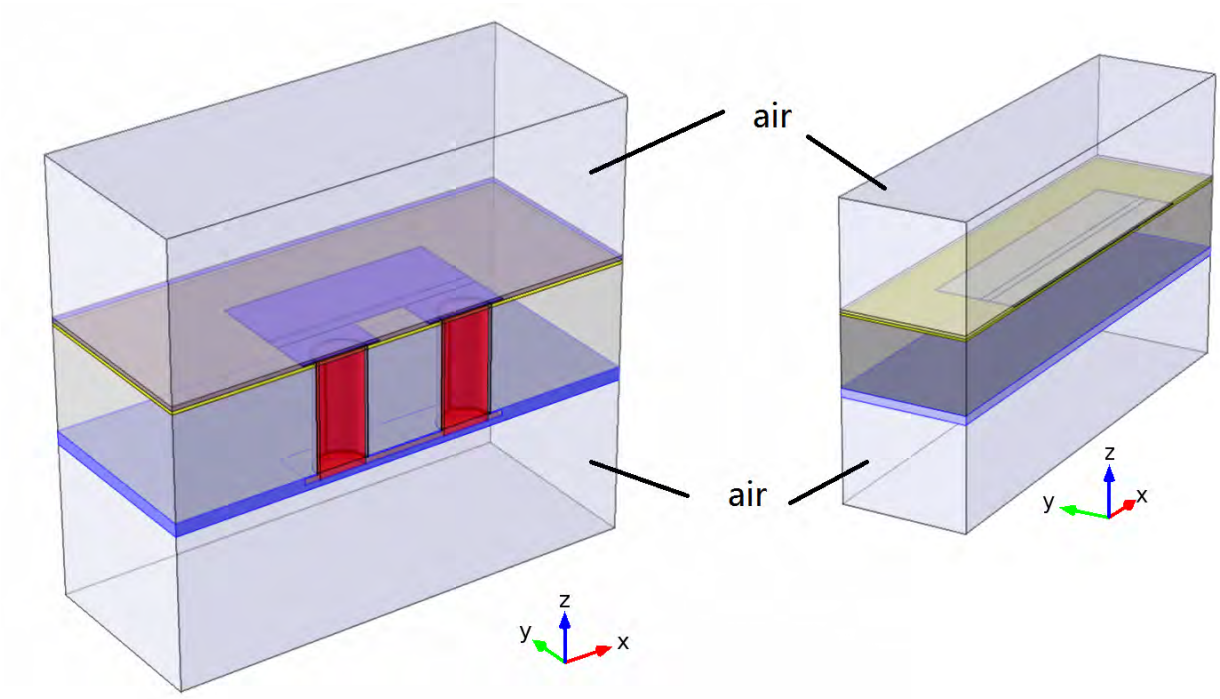


Figure 4-27 Air domain setting

4.4.3.3 Boundary setting

Now we start to set the boundary condition which contains the setting of Port boundary and the type of all outside boundary.

d) Scattering Boundary Condition

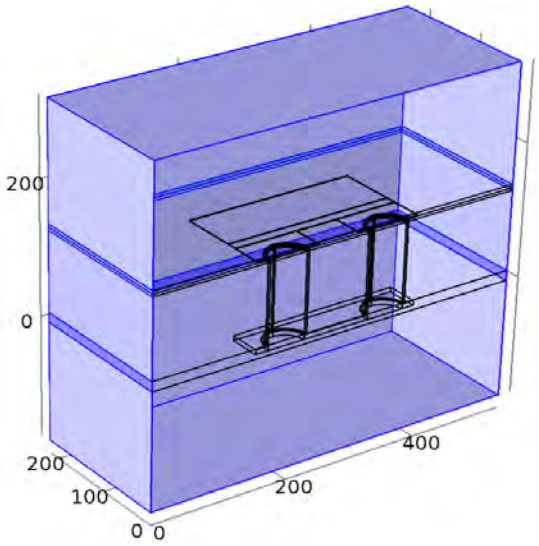


Figure 4-28 Scattering Boundary Condition

We set the outside surface boundary as “Scattering Boundary Condition”.

Actually there is a more suitable boundary condition called “Perfectly Matched Layers (PML)”. “The Perfectly Matched Layers feature is used to set up perfectly absorbing domains as an alternative to low-reflecting boundary conditions. It imposes a complex-valued coordinate transformation to the selected domain that effectively makes it absorbing at a maintained wave impedance thus eliminating reflections at the interface.” But it needs more

memory space and times than the Scattering Boundary Condition. I have compared the result between these two boundary conditions, in our model, the difference is very little, and so I choose the Scattering Boundary Condition. [141]

A PML is not, strictly speaking, a boundary condition but an additional domain that absorbs the incident radiation without producing parasitic reflections. It provides good performance for a wide range of incidence angles and is not particularly sensitive to the shape of the wave fronts. The PML formulation can be deduced from Maxwell's equations by introducing a complex-valued coordinate transformation under the additional requirement that the wave impedance should remain unaffected.

And specially, the PML region is designed to model uniform regions extended "toward infinity". Avoid using objects with different material parameters or boundary conditions that influence the solution inside a PML region. [142]

e) Lumped Ports setting,

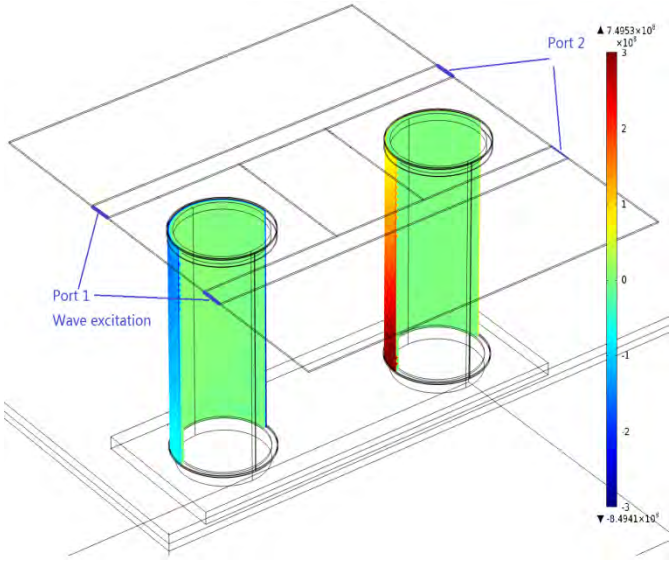


Figure 4-29 Lumped Ports

The Lumped Ports are set as shown in the picture above. The characteristic impedance is 50ohm for each port.

f) Perfect Electric Conductor

The boundary connected to PORT should be set as "Perfect Electric Conductor" as the blue boundary shown in following figure.

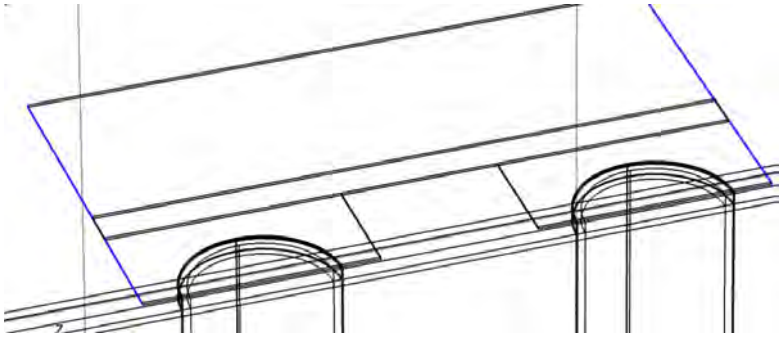


Figure 4-30 Perfect Electric Conductor

g) Symmetric boundary

Due to the symmetric property, we should set the blue “symmetric boundaries” in following figure as “Perfect Magnetic Conductor” with the equation of $\vec{\mathbf{n}} \times \vec{\mathbf{H}} = 0$ and set the white ones as “Perfect Electric Conductor” with the equation of $\vec{\mathbf{n}} \times \vec{\mathbf{E}} = 0$. Use of the symmetric feature of the test structure will decrease the simulation time consumption notably.

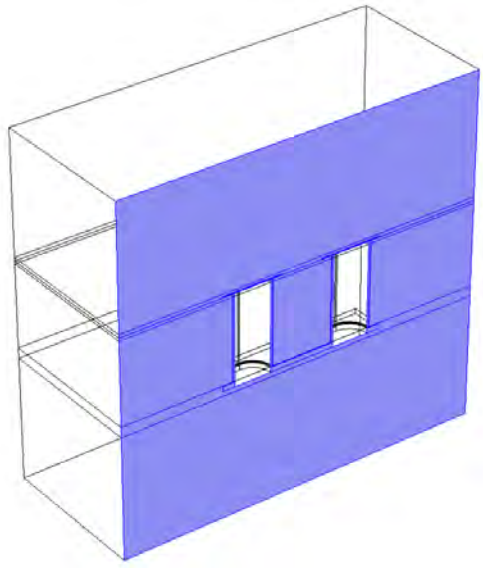


Figure 4-31 Symmetric boundary

4.4.3.4 Mesh setting

The meshes play a very important role in FEM simulation. An optimal mesh leads to the accurate results with least time and memory consumption. Except for the physic control mesh, the manual mesh could also be used. A viable mesh could be created by the Swept Mesh Technology and the Layered Mesh Technology [143]. The mesh may be like in the following figure.

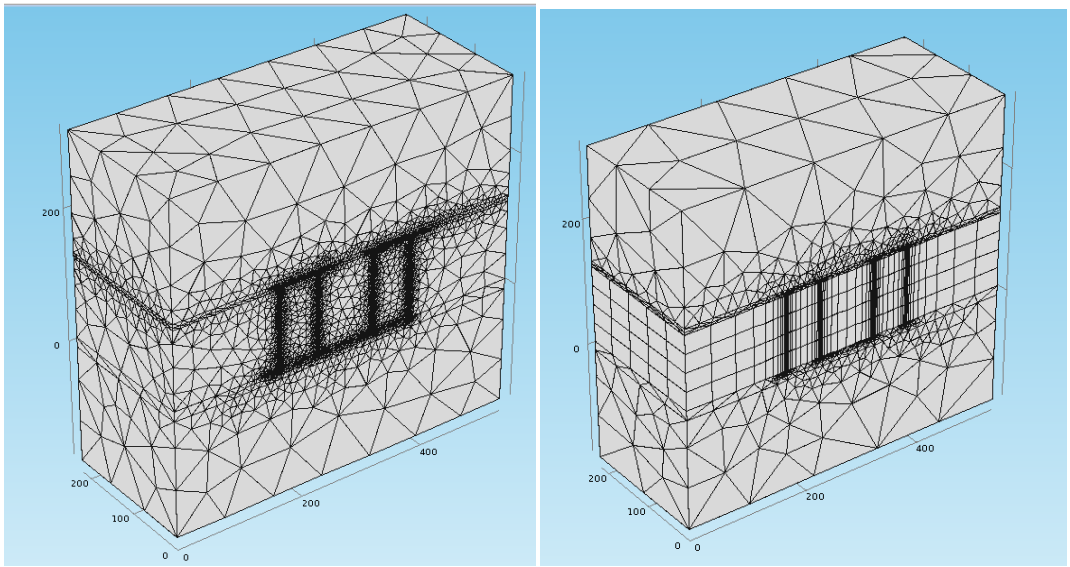


Figure 4-32 Physic control mesh (left) and manual mesh use Swept Mesh Tech (right).

Considered the “Skin Effect” on the outside surface of the TSV, a Layered Mesh could be used on the surface of the TSV in order to improve the accuracy of the result. The layered mesh could produce a very fine mesh on the “near-surface” domain.

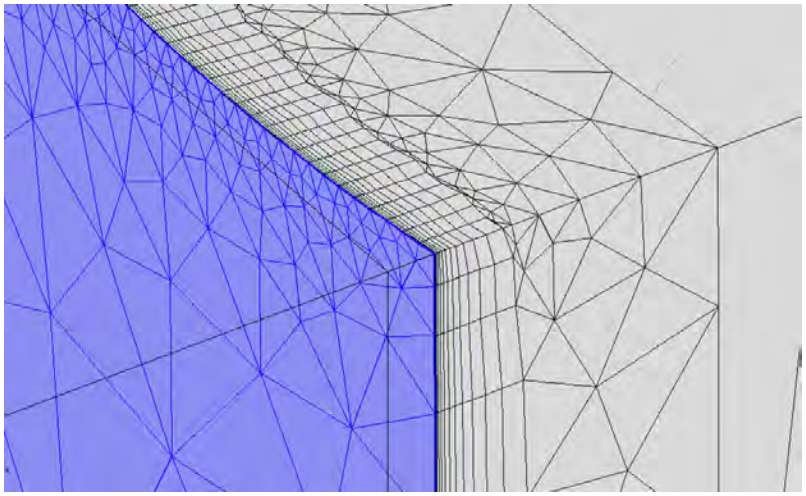


Figure 4-33 Layered mesh on the surface of TSV

4.4.3.5 Some FEM results and analysis

The following figure shows us the Current density and the magnetic field distribution in Substrate. The Slice shows the Current Density in Substrate and the Arrow represents the Magnetic Field .j

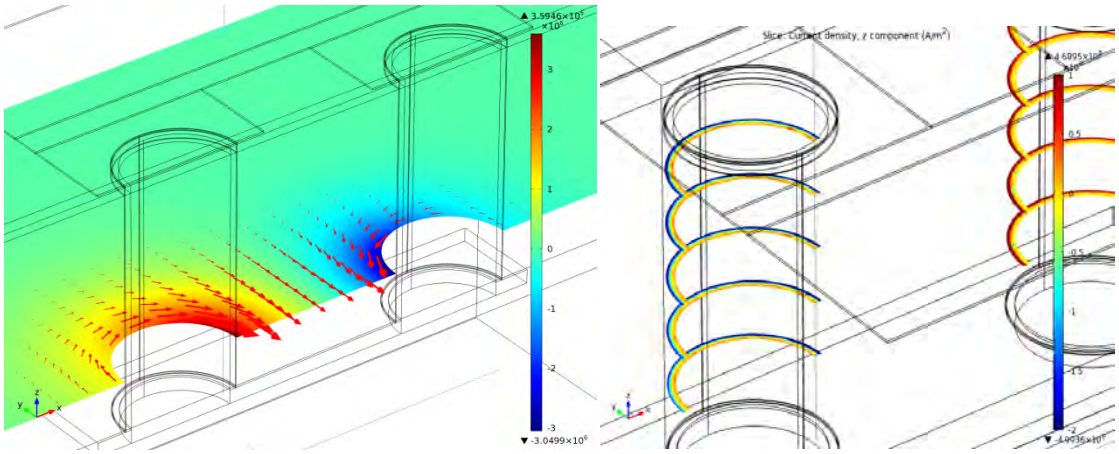


Figure 4-34 Current density and the magnetic field distribution and skin effect

We can also see the inner surface of the TSV has hardly any current, that’s caused by the “Skin Effect”[144]. The Figure 4-34 shows this effect clearly.

4.4.4 Experiment results and compact models results

4.4.4.1 Results for the simple CPW structure

For the first simple CPW structure (c.f. Figure 4-16), the experiment results and ADS simulations results in S parameters are shown in

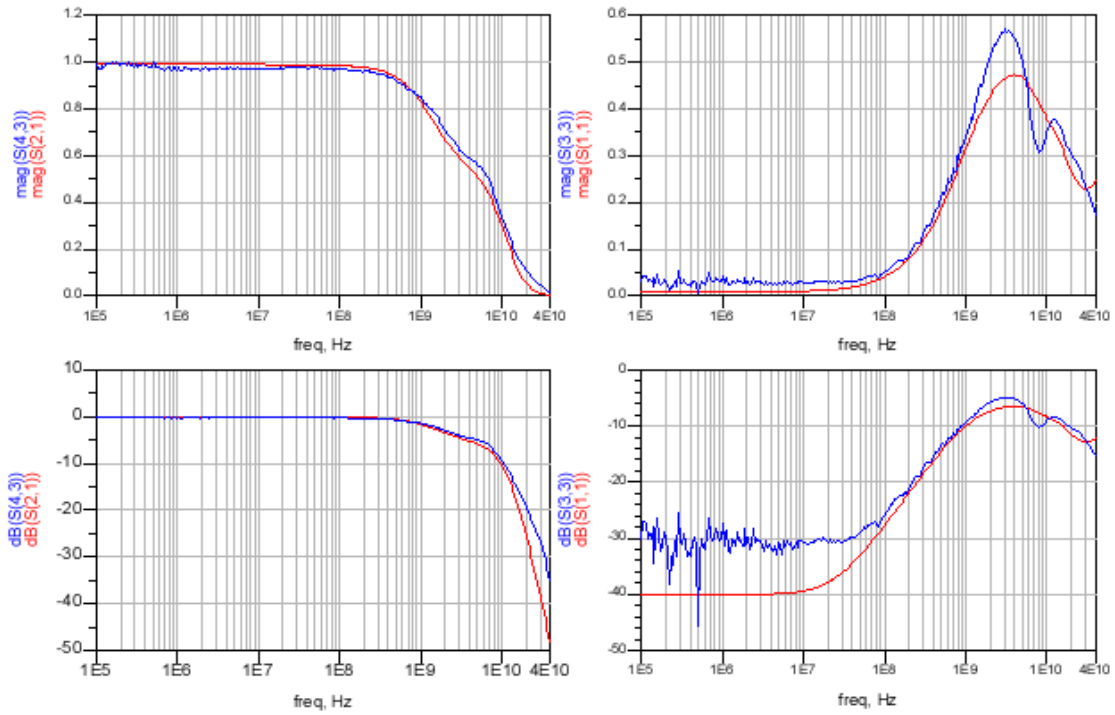


Figure 4-35. The blue lines are the experiment results and the red ones are the results from 3D-TLE/ADS simulation.

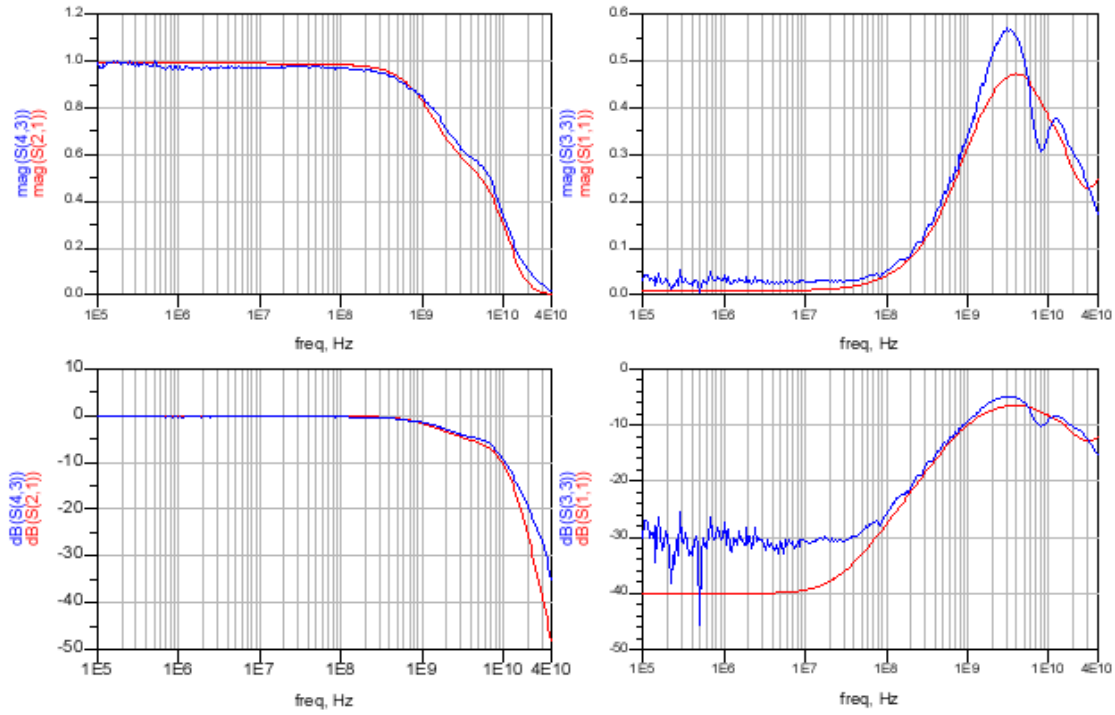


Figure 4-35 S parameter for the simple CPW structure (S21 left; S11 right)

We use the optimizing of ADS, which attempts to have the “best” set of parameter; the difference after ~5GHz frequency is caused by the parameters depend on the frequency (high frequency parameter capacitance, skin effect); then we have to refine our model beyond the 5GHz frequency.

The potential distribution of this structure is also investigated under COMSOL. Figure 4-36 gives the potential distribution upon and below the oxide layer respectively.

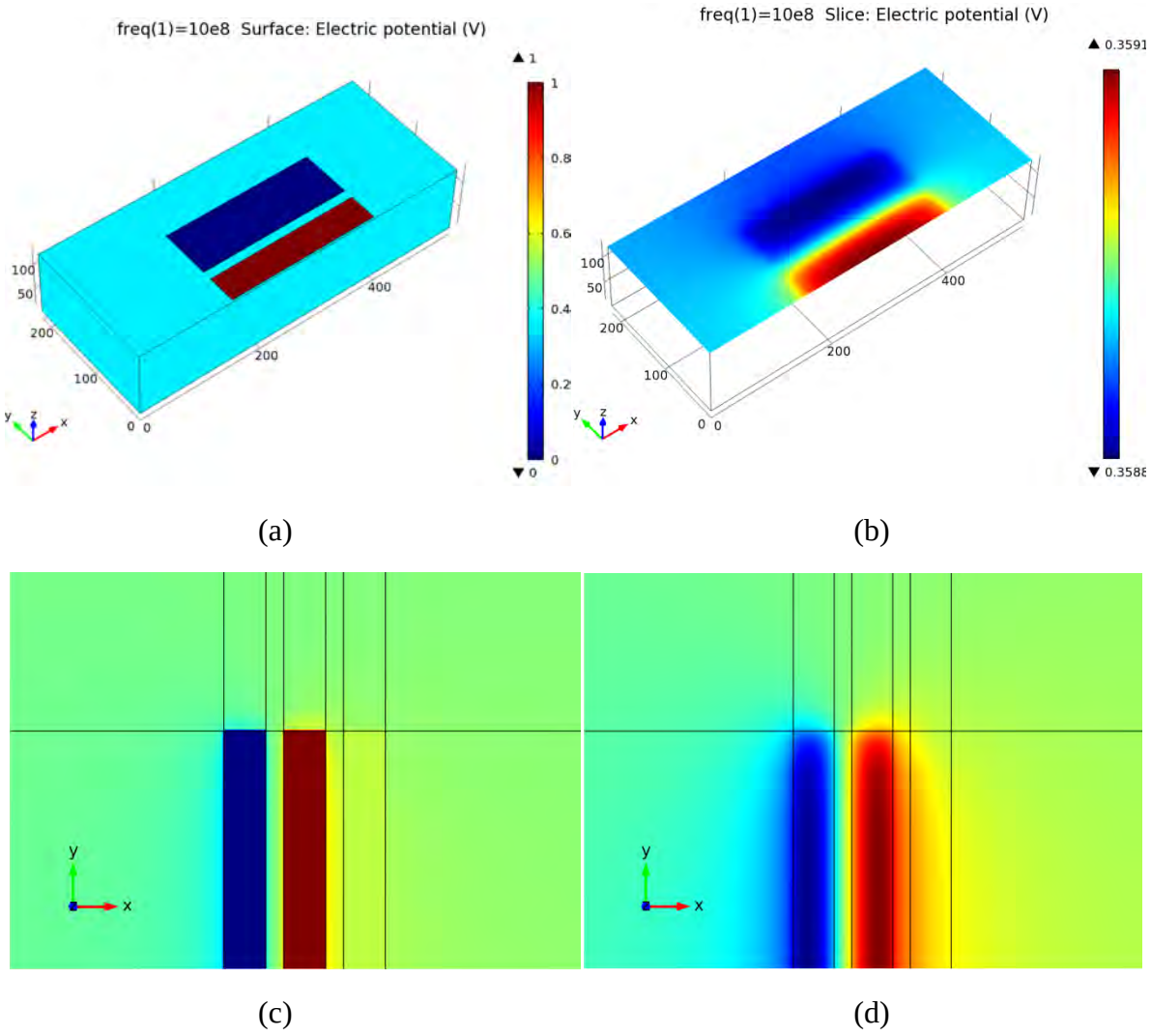


Figure 4-36 Potential distribution upon the oxide layer (a) (c) and below the oxide layer (b) (d) (from COMSOL)

From the result one can find, although the potential upon of the oxide layer is uniform, the potential under the oxide layer (i.e. top of the substrate) is no uniform. That’s why we don’t use a constant voltage on calculating the substrate impedance in Chapter 3.

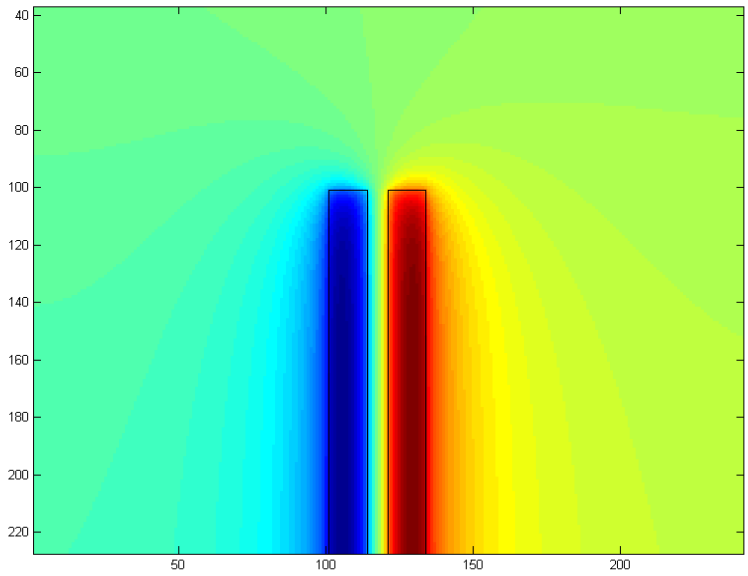


Figure 4-37 Potential distribution below the oxide layer from 3D-IE

A potential distribution below the oxide layer calculated from 3D-IE for the same structure is shown as above (Figure 4-37).

Compare Figure 4-37 with Figure 4-36 (b) and (d), we can find the 3D-IE result is well correspondent to the COMSOL result. And this also proves the use of constant current method is more accurate than the constant voltage method on the top of the substrate.

4.4.4.2 Results for the complicated substrate structures for TSV and CPW

For the later structure used to both CPW and TSVs comparison results are presented in from Figure 4-38 to Figure 4-40.

The test structures' RF responses are plotted with dotted blue curves; those of the electrical models with plain red curves. The equivalent RLCG compact models proposed for the coplanar waveguides and the TSV chains demonstrate very good accuracy for frequencies up to 20 GHz and 10 GHz, respectively. Some spikes can be observed in measurements but not in simulations at low frequency (below 1 GHz). These resonances are due to the coupling between the test structure substrate and its measurement environment. The test sample is a piece of metal which acts as an excellent antenna with uncontrolled impedance to the measurement ground. This unknown impedance explains the unexpected poles of resonances. The spikes can be suppressed by isolating the test structure from its environment, implying the substrate has to be strongly grounded or biased.

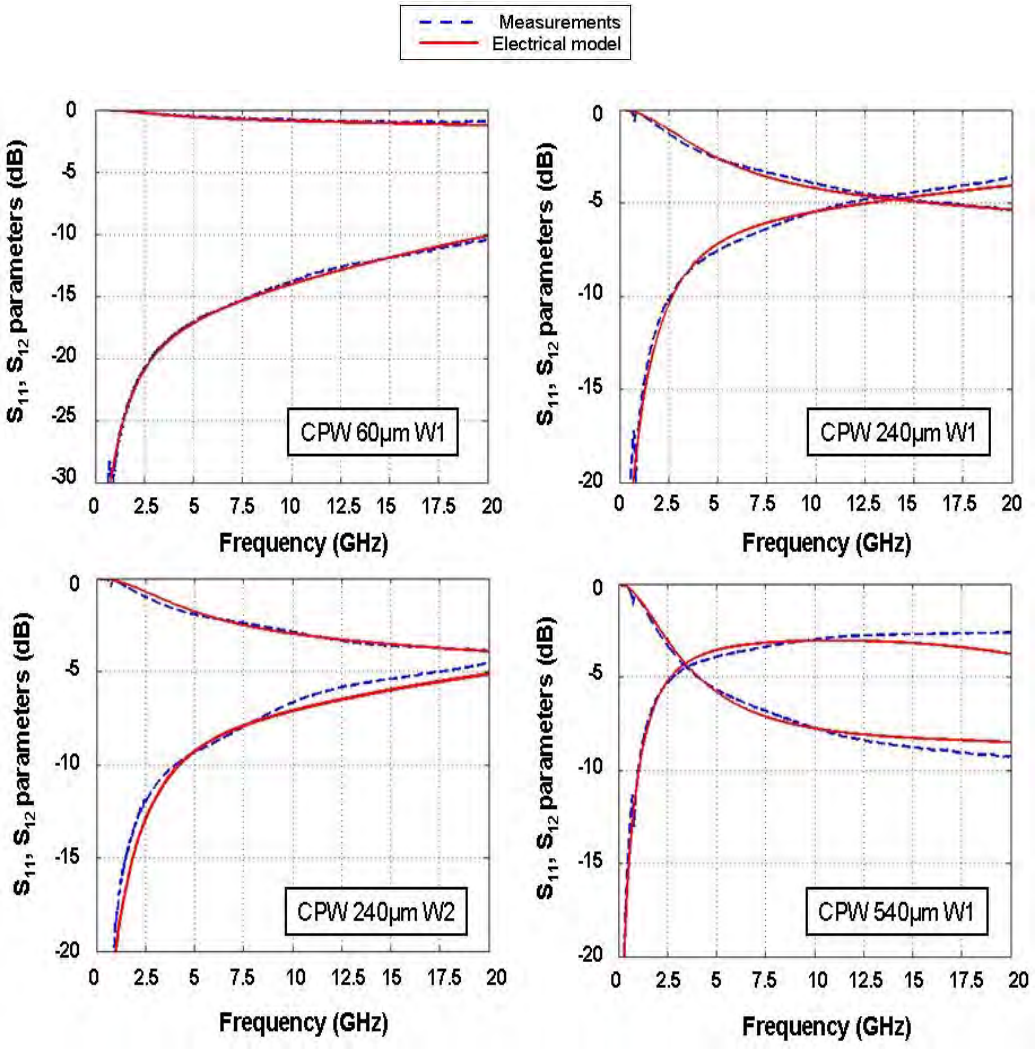


Figure 4-38 S-parameter comparisons, up to 20 GHz, between the measurements performed on coplanar waveguides test structures and the simulations of their electrical equivalent models for both W1 and W2 configurations and different coplanar lines lengths.

The coplanar waveguides in W2 configuration give rise to better transmission resulting from less insertion losses due to higher impedance along the leakage path through the substrate. The signal line width is smaller in this configuration, resulting in a lower oxide capacitance. Nevertheless, the insertion losses are dominated by the coplanar BEOL lines resistive losses which increase for higher line lengths.

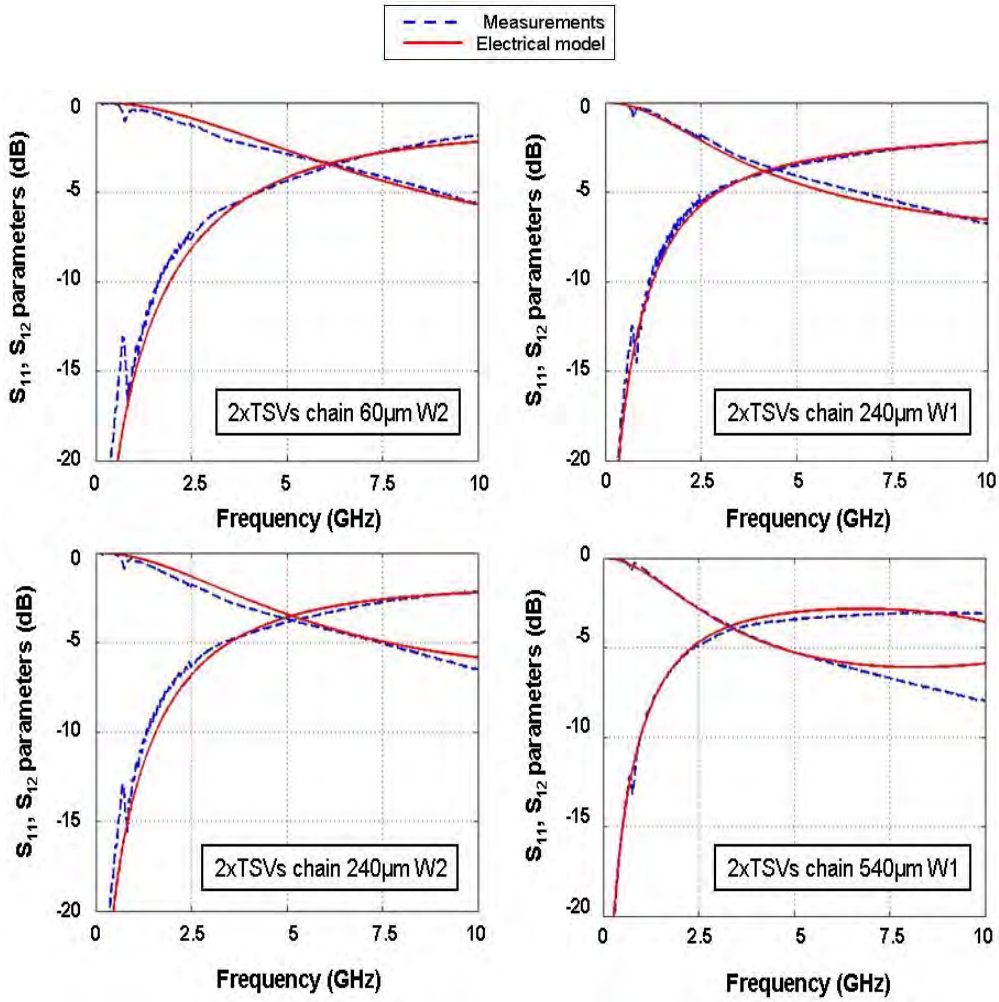


Figure 4-39 S-parameter comparisons, up to 10 GHz, between the measurements performed on 2xTSVs chain test structures and the simulations of their electrical equivalent models for both W1 and W2 configurations and different coplanar and back redistribution line lengths.

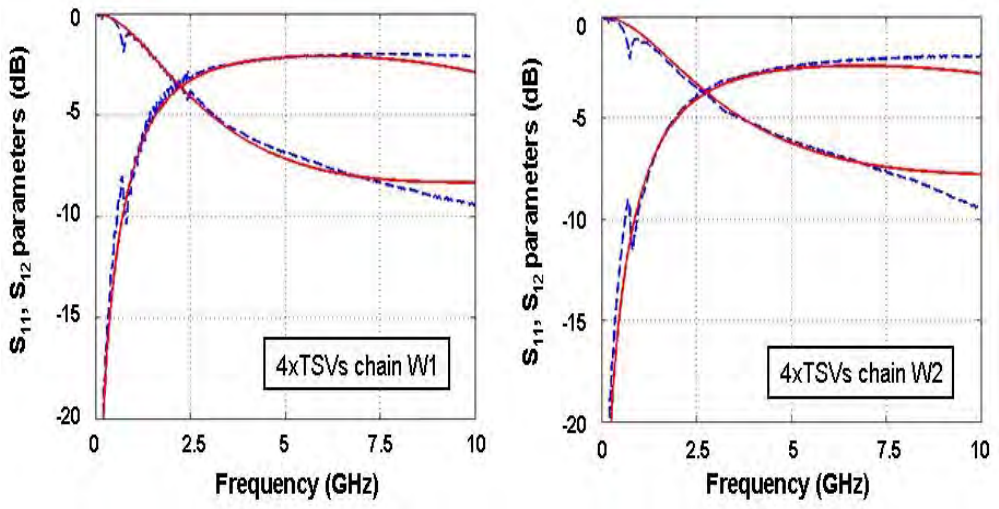


Figure 4-40 S-parameter comparisons, up to 10 GHz, between the measurements performed on 4xTSVs chain test structures and the simulations of their electrical equivalent models for both W1 and W2 configurations.

In the case of the 2xTSV chains, performances, evaluated depending on the insertion losses, are better for low and medium frequencies in W2 configuration. The insertion losses are mainly due to leakages through the substrate via the oxide layer surrounding the TSV

since it forms a MIS (Metal-Insulator-Silicon) capacitor $C_{ox(TSV)}$ with the substrate. It appears from equation(4.11) that this capacitance depends on the oxide and metal layers thicknesses.

The data for the oxide and copper layers in the conic TSVs are imposed by the technology process but the TSV diameter variations from the top to the bottom surfaces are different for the W1 and W2 configurations. The oxide capacitance is smaller in the W2 configuration for which the TSV top and bottom surface diameters are smaller and the variations higher. Therefore, the impedance along the leakage path to the substrate is larger and hence the insertion losses are reduced. The resistive losses from the TSVs themselves are negligible because of the low resistivity of copper (R_{TSV} is equal to a few milliohms for both configurations).

The insertion losses are also due to the resistive losses in the BRDL line. The higher the BRDL line length, the larger the insertion losses. In addition, when increasing in frequency, the insertion losses tend to be dominated by the BRDL line inductive effects, i.e. by the line self inductance. From their geometrical descriptions, the self inductance of the BRDL line in W1 configuration is smaller than that in the W2 configuration. This explains why the 2xTSV chain has better performances in W2 configuration up to a certain frequency and better ones in W1 configuration beyond that point. Depending on the BRDL line length, this point can be reached at medium or high frequency (Figure 4-41).

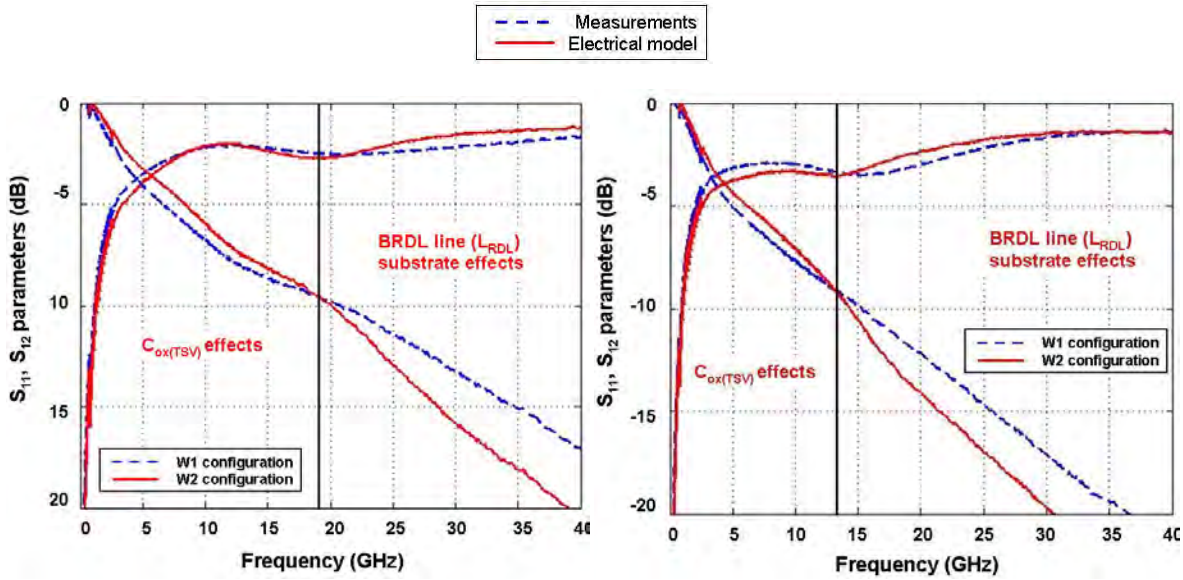


Figure 4-41 S-parameter comparisons for 2xTSVs chains between W1 and W2 configurations. Top: the BRDL line length is 420 µm; the spacing between contact pads at the BEOL level is 240 µm. Bottom: the BRDL line length is 720 µm; the spacing between contact pads at the BEOL level is 540 µm.

In the high frequency range, the estimation error between the test structures' RF responses and the ones of their equivalent electrical models is higher than 10% because the substrate coupling effects are neglected. The substrate extraction method, associated with the modeling approach, is validated here for a coplanar waveguide atop a highly resistive substrate. The S-parameters given by the electrical model have been compared, for a frequency range up to 20 GHz, with the responses obtained from a simulation of the structure realized under a 3D electromagnetic simulator[104]. The results of this comparison are shown on Figure 4-42 for DC substrate electrical modeling. The percentage error in evaluating S_{12} is relatively high as the losses are actually practically negligible, as it can be seen on the figure.

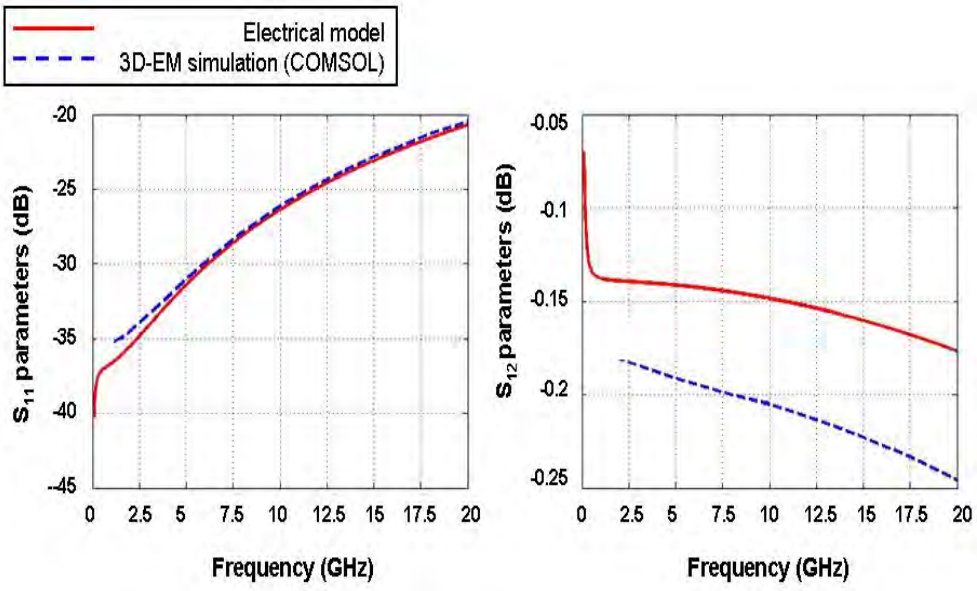


Figure 4-42 S-parameter comparisons for a 240 µm coplanar waveguide system atop a highly resistive substrate. The substrate is modeled with DC parameters electrical parameters. Left: S11 parameters. Right: S12 parameters.

4.5 Conclusion

In this chapter, a compact modeling approach for 3D interconnects is presented, here applied to redistribution lines and medium-density TSVs, based on parametrical extractions performed on realistic test structures, 3D electromagnetic simulations and a Transmission Line Method. The proposed modeling approach includes the system global electrical context such as current paths and the modeling of proximity and/or substrate effects. Complete equivalent electrical models are illustrated for coplanar waveguides and TSV chains structures. The modeling approach is validated through frequency analyses by comparing the S-parameters measured on the test structures with those obtained by simulating their respective equivalent electrical models. The results show some very good accuracy at low and medium frequencies and enable the clear identification of the structure's electrical parameters which impact insertion losses. Nevertheless, the observed errors are more significant at high frequency since we have presently modelled electrically the substrate as a simple node. Indeed, this assumption is only viable when the substrate is highly conductive in low and medium frequency domains. At high frequency, the substrate effects must be integrated into the electrical model as a RLCG network; but the effects, between all the elements sharing the substrate, have also to be modelled. On-going works will consist in extending the modeling approach to other 3D interconnect types, such as copper pillars for which a model has been proposed in [145] but here is without inductive coupling consideration, and to different types of 3D interconnect matrices. The substrate extractor will be incorporated in cases of chains and matrices of TSVs, to electrically model, with increased accuracy, a large panel of 3D structures and critical paths and to investigate signal integrity.

5 Perspective and Future Trends

In this chapter, the perspective and future trends will be introduced. Firstly is the study of signal integrity in TSV matrices. Then the thermal analysis of TSV structure is investigated due to the electro-thermal effect of the TSV. As a consequence of the skin effect, observed in last chapter, the skin effect and eddy current on TSV model will also be analyzed. A first result on signal fluctuations correlation analysis is followed. At last a conclusion for this chapter is stated.

5.1 Study of Signal Integrity in TSV Matrices

A first glance on timing analyses are reported here via Eye Diagrams performed on different TSVs matrix configurations, depending on signal types sent to the TSVs near ends, to investigate signal integrity issues in such 3D structures.

Since the TSV electrical model has been validated in low and medium frequency ranges, timing analyses are proposed using Eye Diagrams to examine the signal integrity in the case of a 3x3 medium-density TSVs regular matrix. We have modeled it considering TSVs having the same dimensions used in their W1 configuration (cf. §4.4). The pitch between the TSVs is equal to 120 µm. The signal integrity is studied at low and medium frequencies; so we make the assumption that all the TSVs oxide capacitances join at a single node representing the substrate. Figure 5-1 shows this modeling consideration for a 2x2 TSVs matrix. Only the proximity effects between all the TSVs (inductive couplings) are once more evaluated in these analyses. The Eye Diagrams are produced by assuming in the simulation a symmetrical test bench with 50 Ω output buffer equivalent resistances connected to each TSV input. The TSVs are terminated with 4fF load capacitances (Figure 5-2).

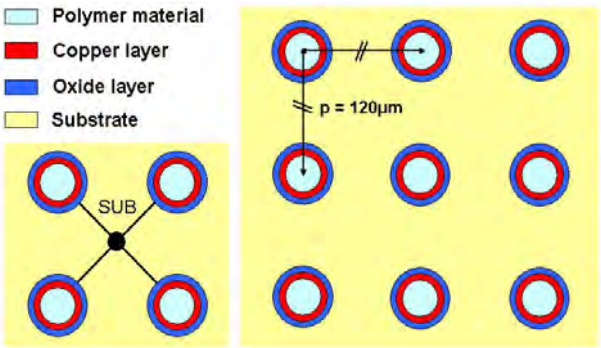


Figure 5-1 Medium-density TSVs regular matrices. Bottom left: all the TSVs' oxide capacitances join at a single node modeling the substrate (illustration for a 2x2 matrix). Right: 3x3 medium-density TSVs matrix considered for the timing domain analyses.

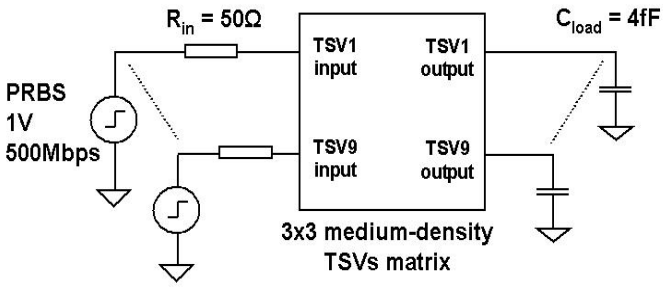


Figure 5-2 3x3 TSV matrix test bench used for Eye Diagram simulations.

Three configurations are investigated and illustrated in Figure 5-3. For the first one, all the TSVs are grounded except the central TSV. The second configuration is a shielded arrangement for which data is transmitted through the matrix's inner TSVs; the outer ones are grounded. In the third configuration, data is transmitted to all the TSVs.

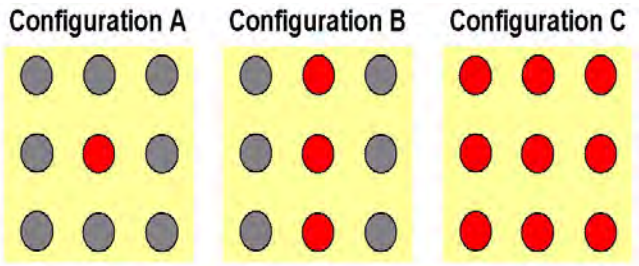


Figure 5-3 3x3 medium-density TSV matrix configurations for generating Eye Diagrams from simulations. Color legend: grey for grounded TSV, red for signal. Configuration A: data is only transmitted through the matrix central TSV. Configuration B: shielded configuration. Configuration C: data is sent to all the TSVs.

The simulation-generated Eye Diagrams are presented in Figure 5-4. When signals propagate in a "guilty" TSV, crosstalk voltages can be observed on a coupled neighboring "victim" TSV which is at a logic state (configuration A or B). A propagation delay can also be observed if the victim TSV transmits a signal as well. The larger the pitch between two coupled TSVs, the more the proximity effects can be neglected. The performance degradation due to the inductive coupled effects can be clearly observed in the B and C configurations.

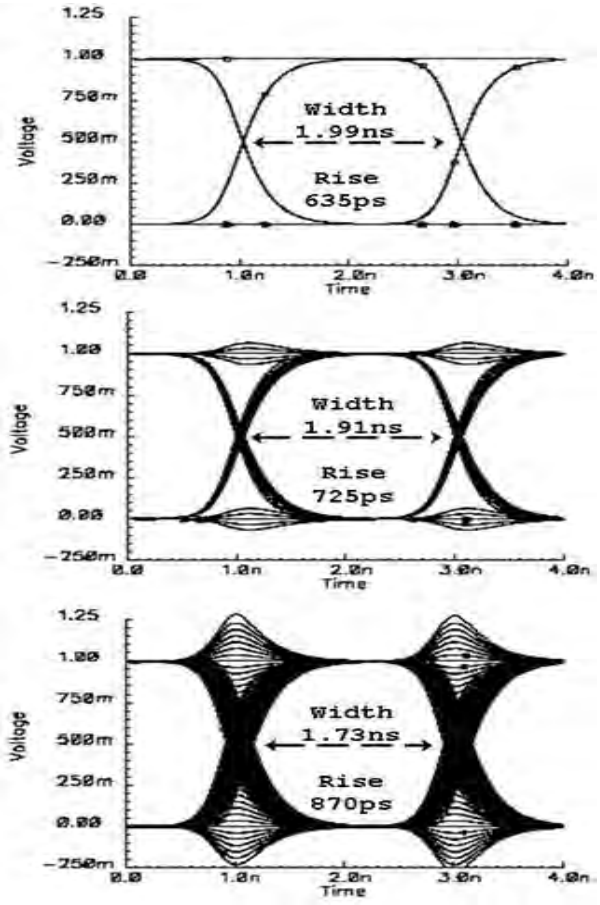


Figure 5-4 Generating Eye Diagrams from simulation based on the three studied configurations. TOP: A configuration. Middle: B configuration. Bottom: C configuration.

As the number of neighbouring TSVs carrying data increases, the rise time, and hence the propagation delay, increases. Consequently, the eye width is shortened. In comparison to configuration A, the rise time in configuration C is 37 % longer. Additionally, the voltage overshoot linked to the crosstalk ranges from 65 mV up to 250 mV in the B and C configurations, respectively. As the noise margins decrease with technological evolution, signal integrity in TSV matrices must be more fully quantified for cases in which signals propagate in the same direction, as in the presented analyses, or in opposite directions. The couplings between the TSVs and the substrate must also be integrated into the TSVs matrices' electrical models to evaluate what kind of coupling has the most impact on structure performances and signal integrity.

The results show that the 3D-TLE extractor can be easily integrated with a common EDA environment by providing compact models capable of analyzing the performance of TSVs bundles for high speed data communication.

5.2 Thermal analysis of TSV structure

In 3DICs, heat dissipating devices have a higher heat density than in a comparable 2D chip as, a consequence of stacking devices directly on top of each other. So the thermal model should also be extracted.

5.2.1 Thermal model of TSV

A TSV Kelvin structure in [146] as shown in Figure 5-5 is used to measure the TSV resistance.

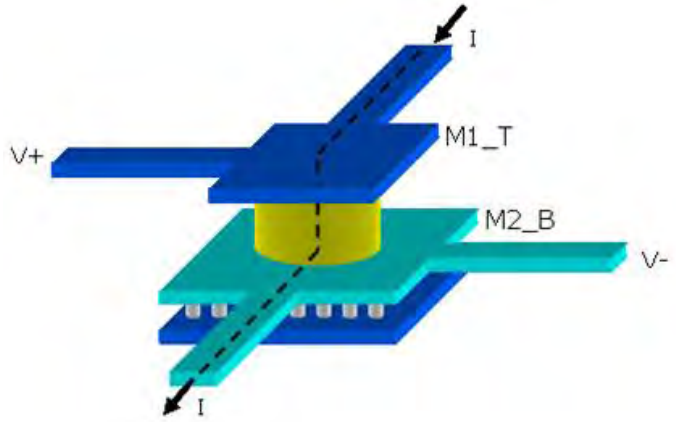


Figure 5-5 TSV Resistance Measurement Structure [146]

The corresponding resistance variations with increasing temperatures are shown in Figure 5-6.

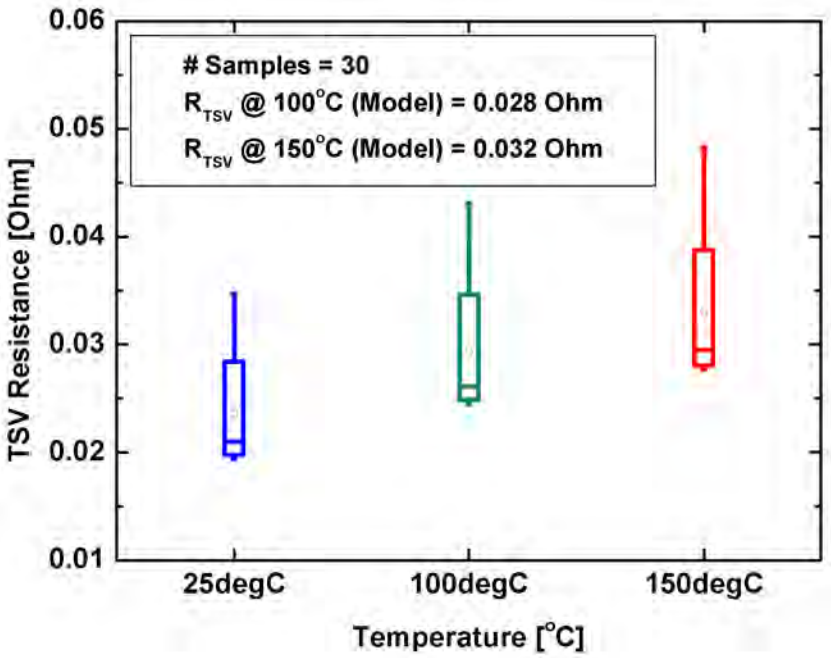


Figure 5-6 TSV resistance variation with temperature [146]

As consequence, an empirical temperature dependent TSV RC model is proposed in Figure 5-7.

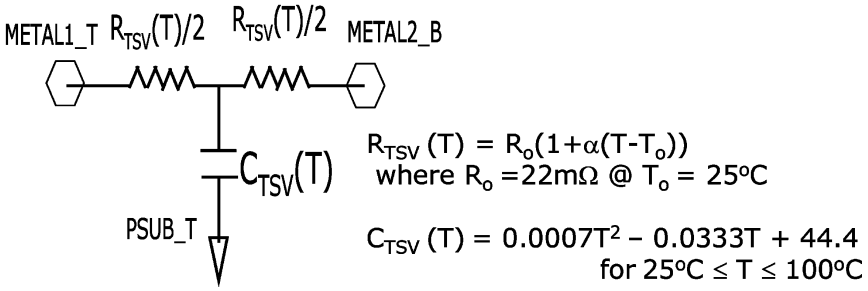


Figure 5-7 Empirical temperature dependent TSV RC Model [146]

Reference [147] presents a new methodology and its applications to accurately and efficiently predict power and temperature distribution for 3D ICs. Figure 5-8 is a 3D view of temperature profiles in SRAM + TSVs + SoC There are 100 TSVs of 0.1mm in diameter connecting the two chips.

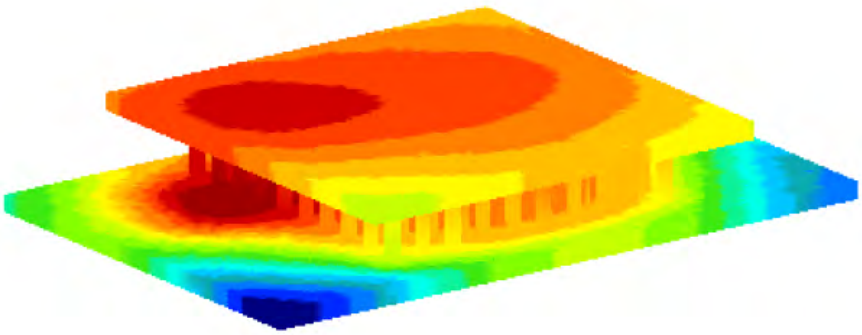


Figure 5-8 Temperature on SRAM+TSVs+SoC [147]

Three Green function based thermal simulation algorithms for calculating the on-chip temperature distribution in a multilayered substrate structure are represented in[148] and [149]. But it is not applied for TSV structures. In [150], thermal models were employed to evaluate the rise in temperature of metal interconnects on the surface of substrate, where the lateral heat dissipation was taken into account for different spacing between two interconnects.

A simplified total lumped model of a temperature-dependent TSV-TSV structure is shown in Figure 5-9. [52]

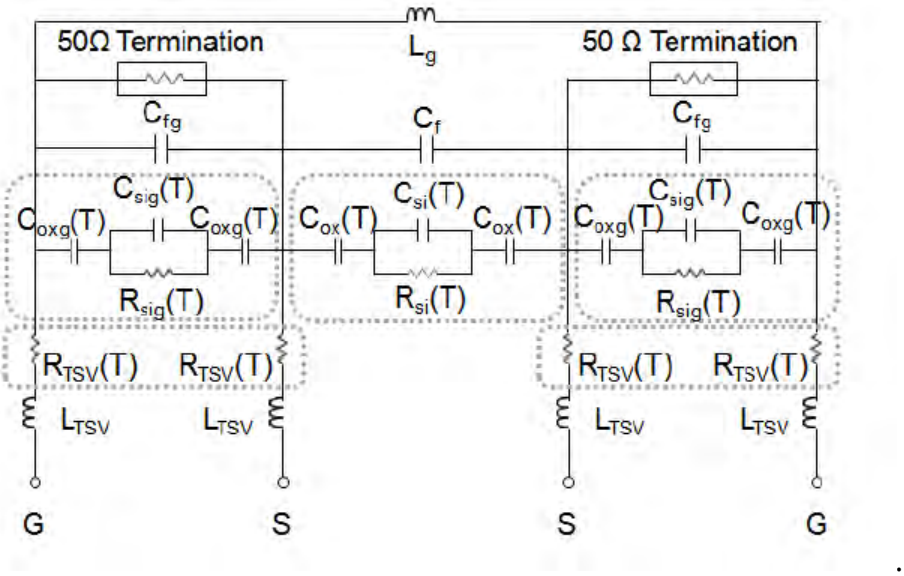


Figure 5-9 Simplified total lumped model of a temperature-dependent TSV-TSV structure. The components inside the dotted circle are temperature dependent. Small parasitic components are omitted.[52]

5.2.2 Electro-thermal simulation of TSV

Combined with a thermal network or behavioral model of the stacked structure, a coupled electro-thermal analysis of the entire system is necessary. [100, 151, 152] Figure 5-10 shows the basic flow of coupled electro-thermal analysis of a system.

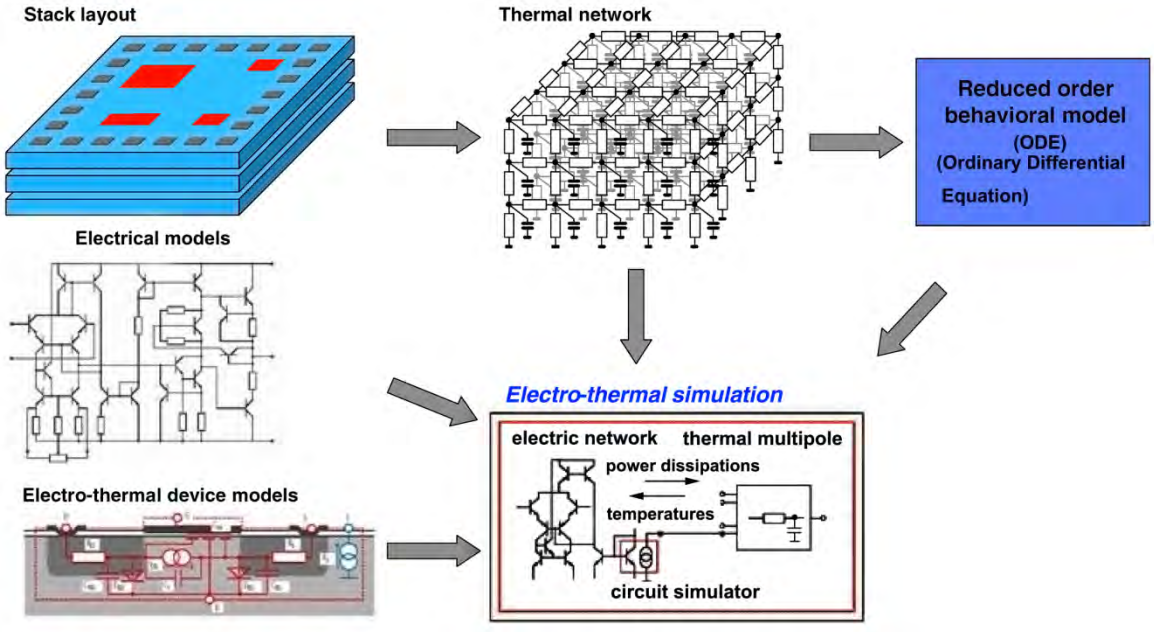


Figure 5-10 Basic flow for electro-thermal simulation[100]

An accurate electro-thermal model is necessary for the extraction of TSV feature in the future due to the electro-thermal coupling effect.

5.3 Skin and proximity effect on TSV model and Eddy Current

As we have discussed in chapter 4, from Figure 5-11, we can see the inner surface of the TSV has hardly any current, that's caused by the "Skin Effect"[144] of the TSV. The proximity effect can also been observed.

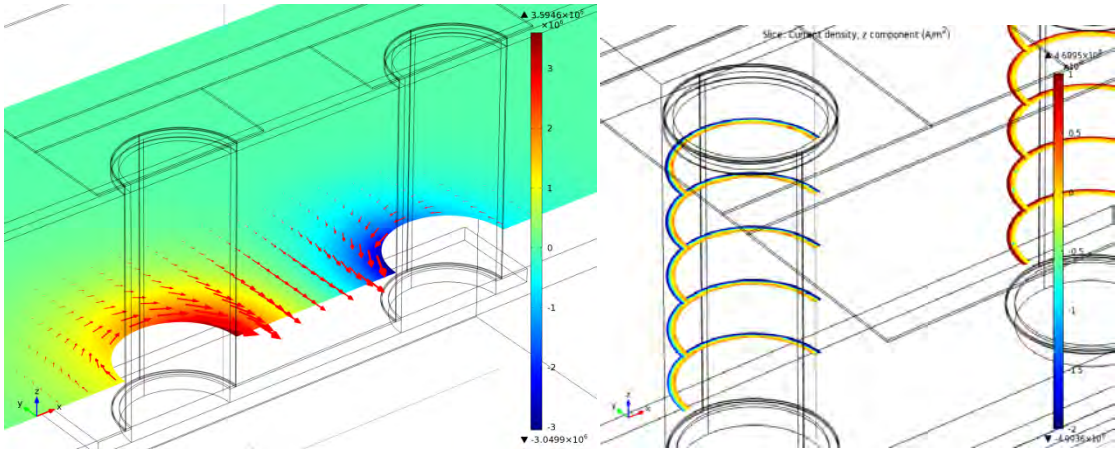


Figure 5-11 Current density and the magnetic field distribution and skin effect

In normal cases, the skin depth is well approximated as[153]:

$$\delta_{\max} = \sqrt{\frac{2}{\sigma \omega_{\max} \mu}} \tag{5.1}$$

where σ = conductivity of the conductor

ω = angular frequency of current

μ = absolute magnetic permeability of the conductor

So, the skin effect is essential to treat the pair R, L over a broad frequency spectrum for some realistic diameter of the TSVs.

5.3.1 Skin effect and proximity effect TSV model

To model accurately, the skin depth of TSV, δ_{tsv}, is considered in the calculation of R_{tsv}; it affects from frequencies above 20 MHz and has a 16 times larger resistance at 20 GHz compared with the dc resistance.[154]

$$\begin{aligned} R_{\mathrm{TSV}} &= \frac{1}{2}\frac{1}{\sigma_{\mathrm{TSV}}}\frac{h_{\mathrm{unit}}}{\pi r_{\mathrm{TSV}^2}}\ [\Omega]\ \left(if\ \ \delta_{\mathrm{TSV}} \geq r_{\mathrm{TSV}}\right) \\ R_{\mathrm{TSV}} &= \frac{1}{2}\frac{1}{\sigma_{\mathrm{TSV}}}\frac{h_{\mathrm{unit}}}{\pi\left(r_{\mathrm{TSV}}^2 - \left(r_{\mathrm{TSV}} - \delta_{\mathrm{TSV}}\right)^2\right)}\ [\Omega]\left(if\ \ \delta_{\mathrm{TSV}} < r_{\mathrm{TSV}}\right) \end{aligned} \tag{5.2}$$

where $\delta_{\mathrm{TSV}} = \frac{1}{\sqrt{\pi f \mu \sigma_{\mathrm{TSV}}}}[m]$ is the skin depth.

As in reference [155], in addition of skin effect, there is another effect that induces current flow on the surface of the conductor, but is no uniformly distributed around the perimeter by attracting currents to the inside-facing surfaces of the conductors, so called “proximity effect” So the author proposed a formula as followed,

$$R_{\mathrm{TSV}} = \sqrt{\left(R_{\mathrm{dc,TSV}}\right)^2 + \left(R_{\mathrm{ac,TSV}}\right)^2} \tag{5.3}$$

Where,

$$R_{\mathrm{dc,TSV}} = \rho_{\mathrm{TSV}} \frac{h_{TSV}}{\pi \cdot \left(d_{\mathrm{TSV}} / 2\right)^2} \tag{5.4}$$

$$R_{\mathrm{ac,TSV}} = k_p \left(\rho_{TSV} \times \frac{h_{TSV}}{2\pi \times \frac{d_{TSV}}{2} \times \delta_{\mathrm{skin\ depth,TSV}} - \pi \delta^2_{\mathrm{skin\ depth,TSV}}} \right) [\Omega] \tag{5.5}$$

$$\delta_{\mathrm{skindepth,TSV}} = \frac{1}{\sqrt{\pi f \mu_{\mathrm{TSV}} \sigma_{\mathrm{TSV}}}} [m]$$

k_p is the proximity factor, it increases as round conducting wires such as TSVs are brought closely together. The magnitude of the proximity factor is determined by the ratio of p_{TSV} / d_{TSV} . The p_{TSV} is the TSV-TSV pitch and d_{TSV} is the diameter of TSV.

5.3.2 Eddy Current

In the high frequency simulation of contact to contact model in Chapter 3, an eddy current in silicon is observed. For the horizontal interconnects, an approximate way is to use the approximate complex image method described in [156]. So for TSV, the eddy current should also be considered in high frequency. The current between two contacts lied in Layer 4 and Layer 8 used a Constant Voltage method is shown in following figure. The substrate used exactly same one with in chapter 3.

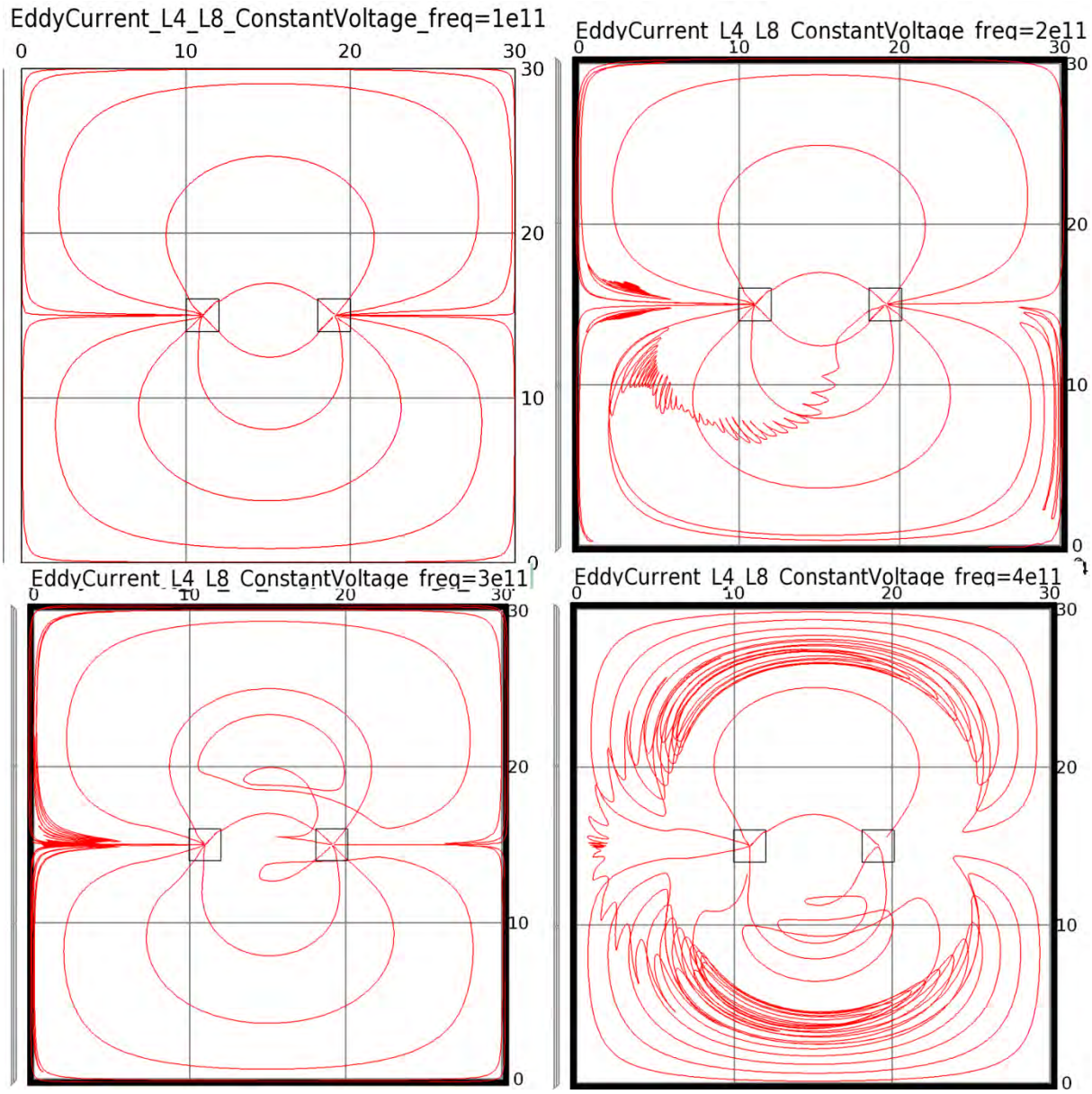


Figure 5-12 Current between two contacts under different frequency

From the Figure 5-12, one can see the eddy current can be observed from about 200GHz (be aware in the bottom right figure, we are going out the quasi-static region). So in future trends, the eddy effect should be added to the model to extract the coupling more accurately.

5.4 First results on signal fluctuations correlation analysis

As we suggested, this method ("Green/TLM ") can be linked to the so called impedance transfer method [157-159], considering signal fluctuations; injecting a non-uniform current at a contact can create a potential variation at any another contact. This way, we could analyze possible correlations between different ab initio independent noise sources, for instance considering the nano-scale.

Use the same model as in §3.3.2, now, we consider a non uniformity of the current density under an" aggressor "contact (L_4/L_5: e.g. capacitive effects at low frequencies).

Calculating the average potential Va under the all "aggressor" contact surface (20*20 points), we can derive a varied I current at each of the 400 points (i=1 to 400) of this contact by the ratio of (Vi-Va) over the impedance from each i contact point (Substitution theorem).

Now the current I at the L_4/L_5 can induce some potential fluctuations, at another probing contact (here: in L_8/L_9). On Figure 5-13 presented are the potential all over the die, respectively for a frequency of 3 GHz (a) and 300 GHz (b) and, on the Figure 5-14 the non uniform injected current at the source contact in L_4/L_5, respectively for a frequency of 3 GHz (a) and 300 GHz (b)

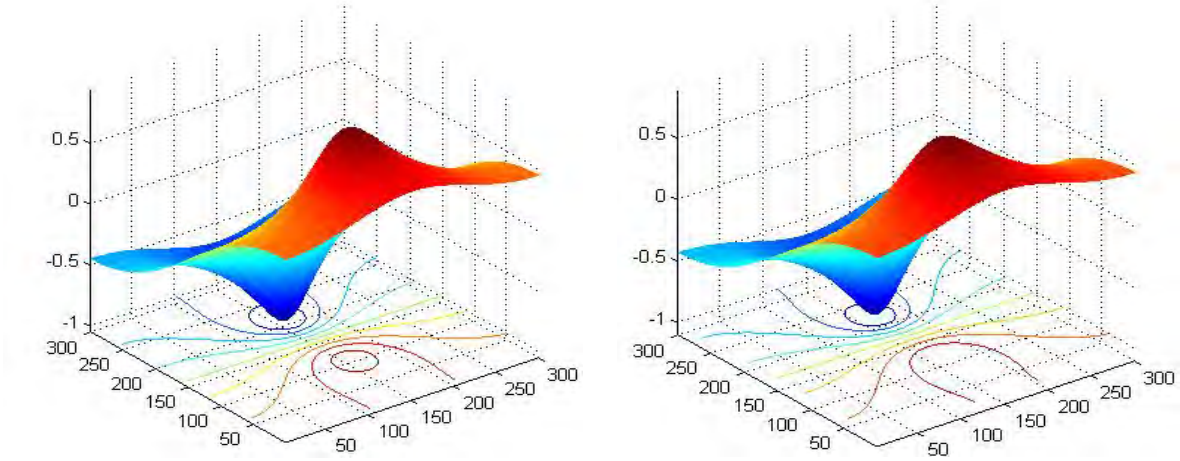


Figure 5-13 cf. § 3.3.2: (a) normalized voltage map at 3GHz; (b) normalized voltage map at 300 GHz - source current density constant

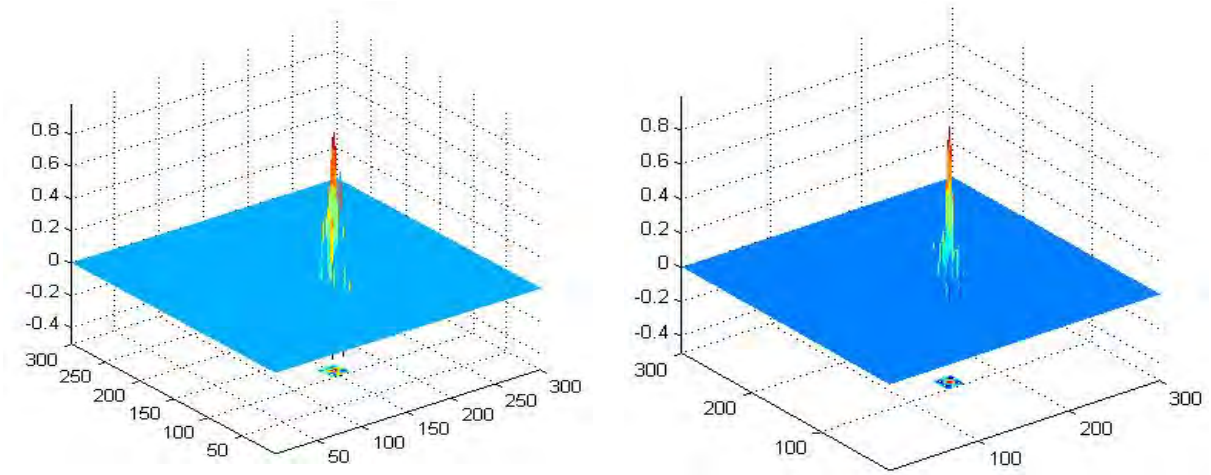
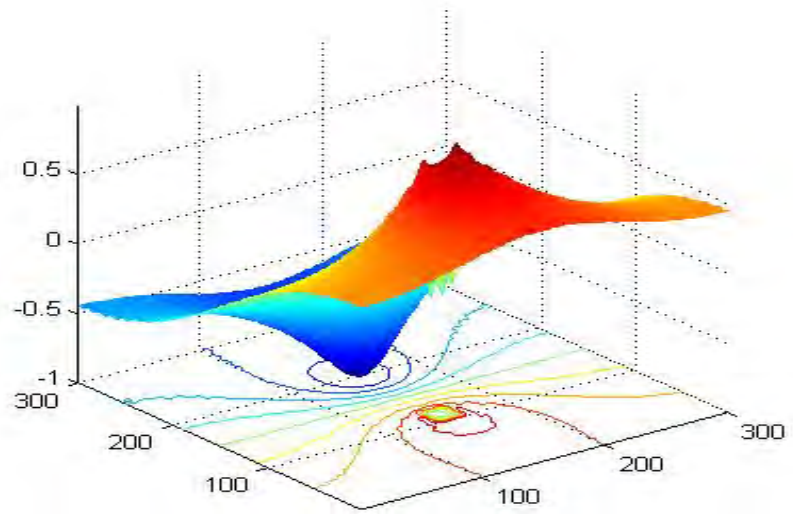
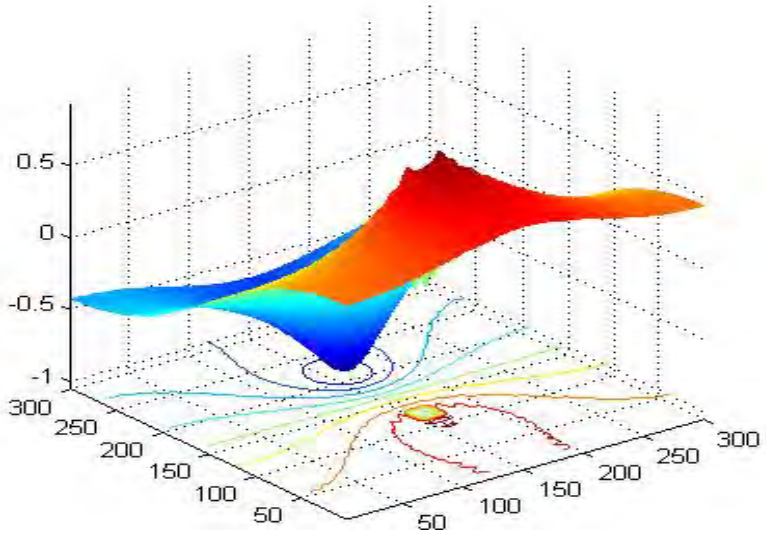


Figure 5-14 cf. § 3.3.2. Source contact current (normalized) - density non constant- (a) located at L_4/L_5 at 3GHz; (b) located at L4/L5 at 300 GHz.



(a)



(b)

Figure 5-15 The deduced normalized potential (current density: non constant –see fig. 5-14): (a)in the pass band 3 GHz, (b)at very high frequency: 3×10^{11} Hz. (c.f. § 3.3.2)

In the first case (into the pass band), we can observe that the projected equipotential curves at the ”target” contact (low potential region) are not smooth but festooned, at the difference of those of Figure 5-14(b) (at a very high frequency). This qualitative result seems us important and merits some future trends in a noise point of view.

The noise behavior of bulk CMOS circuits is dominated primarily by two noise sources: thermal noise and flicker (1/f) noise [160-162], but also sometimes present in the noise spectrum are shot noise, generation/recombination noise, and random telegraphic (popcorn) noise. These sources, at least thermal noise and shot noise, are physically fundamental to the operation of circuits (and devices)

The transfer impedance method (TIM), a proper two-point internal response function, which gives a linear relation between the electric-field or potential response and a local current perturbation, thus, enables one to compute the internal field noise spectra originated from current fluctuations. This method, by generalizing the original impedance field method of Shockley et al [157-159], has been widely used during the last decades for noise calculations, but in one dimension. The essential role of the TIM was, and actually is, to calculate the total spectrum of voltage fluctuations between the terminals of a one-port device.

Currently, no new insights permit to solve this problem in 3D, not because of numerical difficulties, but in a sound physical point of view.

6 General Conclusion

A state of the art in 3D integrated circuit is firstly introduced. 3D architectures for IC integration are a promising alternative to standard 2D designs, when increasing interconnect densities and rising cost of (IC) manufacturing. The challenge encountered in 3D and the fabrication technologies of TSVs are also investigated. Classical methods for substrate noise analysis on analog devices are introduced.

Then, we propose a new substrate network extraction technique based on a Transmission Line Methods or Green kernels that applied for 3D circuits. The substrate coupling and loss in Integrated Circuits can be analyzed by this technique; it could be used to metal contacts or/and Through Silicon Via (TSV), in any number, and they can be placed anywhere into the substrate, or onto; we think this point is somewhat original, up to our knowledge. This feature makes our technique very suitable for the multi-layer substrate. Then, proposed model is verified by Z-parameter simulations using 3D finite element analysis software and analyzed with various parameters: frequency, distance between contacts/TSV and silicon substrate properties. Good fits are also obtained comparing with experiment. As we said, we are very aware that the quasi-electrostatic modeling framework is not valid up to 10 THz (versus experiments), which implies a wave length of roughly ten um in Si; this wave length is of the same order of the contact-to-contact distance (a few um); it is not realistic to go beyond 200 or 300 GHz in these analysis; but we think it is worthwhile to compare with the element finite method to test the robustness of our algorithm.

A compact modeling approach for 3D interconnects is presented, here applied to redistribution lines and medium-density TSVs, based on parametrical extractions performed on realistic test structures, 3D electromagnetic simulations and a Transmission Line Method. The proposed modeling approach includes the system global electrical context such as current paths and the modeling of proximity and/or substrate effects. Complete equivalent electrical models are illustrated for coplanar waveguides and TSV chains structures. The modeling approach is validated through frequency analyses by comparing the S-parameters measured on the test structures with those obtained by simulating their respective equivalent electrical models. The results show some very good accuracy, up to 20 GHz and enable the clear identification of the structure’s electrical parameters which impact insertion losses. Nevertheless, the observed errors are more significant at very high frequency, since we have presently modelled electrically the substrate as a simple node. Indeed, this assumption is only viable when the substrate is highly conductive in low and medium frequency domains. At high frequency, the substrate effects must be integrated into the electrical model as a RLCG network, but the effects between all the elements sharing the substrate have also to be modelled. In addition, the substrate can be non uniform. This is the reason why we also propose a substrate extraction method, relying on the TLM over multi-layered substrates and on the Green functions, to model these effects (the heart of our work). The method efficiency has been tested for contact pads and coplanar waveguides structures and TSVs.

Improved model and several future working directions concerning the research on 3-D IC are then proposed. The analysis in thermal effect, skin, eddy current effect and source noise coupling analysis are also presented.

To conclude, this work can, I hope, in addition to exploring a number of tracks and raise many questions, clarify the features and coupling noise processes involved in contacts, interconnections and TSVs. But much remains to be done, many trends have been explored.

Extension of this work will concern a more precise model and many questions were raised that require research and developments.

Appendix A

A.1 S-, h-, T-, Y-, Z-, ABCD- Parameter Conversions

All these formula in this section is base on the reference of [109]. The 2-port network shown is representative of that implied in the application of these equations. Basic relationships of voltage and current are given in the table to the right. Many other sources exist on the particulars of 2-port network analysis, so it will not be covered here.

S-Parameters

$$b_1 = S_{11}a_1 + S_{12}a_2$$
$$b_2 = S_{21}a_1 + S_{22}a_2$$

Y-Parameters

$$I_1 = Y_{11}V_1 + Y_{12}V_2$$
$$I_2 = Y_{21}V_1 + Y_{22}V_2$$

Z-Parameters

$$V_1 = Z_{11}I_1 + Z_{12}I_2$$
$$V_2 = Z_{21}I_1 + Z_{22}I_2$$

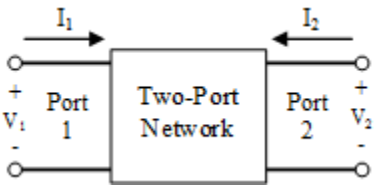
h-Parameters

$$V_1 = h_{11}I_1 + h_{12}V_2$$
$$I_2 = h_{21}I_1 + h_{22}V_2$$

ABCD-Parameters

$$V_1 = AV_2 - BI_2$$
$$I_1 = CV_1 - DI_2$$

All of the parameter equations make use of complex values for all numbers of impedance and the resulting matrix parameters, i.e., Z = R ± jX.



Z_{01} and Z_{02} are the complex impedances of ports 1 and 2, respectively; similarly, Z^*_{01} and Z^*_{02} are the complex conjugates of the respective impedances.

The values R_{01} and R_{02} are the real parts of port impedances Z_{01} and Z_{02}.

S (scattering), Y (admittance), Z (impedance), h (hybrid), ABCD (chain), and T (chain scattering or chain transfer).

S-Parameters from Z-Parameters

$$S_{11} = \frac{(Z_{11} - Z_{01}^*)(Z_{22} - Z_{02}^*) - Z_{12}Z_{21}}{(Z_{11} - Z_{01})(Z_{22} - Z_{02}) - Z_{12}Z_{21}} \qquad S_{21} = \frac{2Z_{21}\sqrt{R_{01}R_{02}}}{(Z_{11} + Z_{01})(Z_{22} + Z_{02}) - Z_{12}Z_{21}}$$

$$S_{12} = \frac{2Z_{12}\sqrt{R_{01}R_{02}}}{(Z_{11} + Z_{01})(Z_{22} + Z_{02}) - Z_{12}Z_{21}} \qquad S_{22} = \frac{(Z_{11} + Z_{01})(Z_{22} - Z_{02}^*) - Z_{12}Z_{21}}{(Z_{11} + Z_{01})(Z_{22} + Z_{02}) - Z_{12}Z_{21}}$$

S-Parameters from Y-Parameters

$$S_{11} = \frac{(1 - Y_{11}Z_{01}^*)(1 + Y_{22}Z_{02}) + Y_{12}Y_{21}Z_{01}^*Z_{02}}{(1 + Y_{11}Z_{01})(1 + Y_{22}Z_{02}) - Y_{12}Y_{21}Z_{01}Z_{02}} \qquad S_{21} = \frac{-2Y_{21}\sqrt{R_{01}R_{02}}}{(1 + Y_{11}Z_{01})(1 + Y_{22}Z_{02}) - Y_{12}Y_{21}Z_{01}Z_{02}}$$

$$S_{12} = \frac{-2Y_{12}\sqrt{R_{01}R_{02}}}{(1 + Y_{11}Z_{01})(1 + Y_{22}Z_{02}) - Y_{12}Y_{21}Z_{01}Z_{02}} \qquad S_{22} = \frac{(1 + Y_{11}Z_{01})(1 - Y_{22}Z_{02}^*) + Y_{12}Y_{21}Z_{01}Z_{02}^*}{(1 + Y_{11}Z_{01})(1 + Y_{22}Z_{02}) - Y_{12}Y_{21}Z_{01}Z_{02}}$$

S-Parameters from h-Parameters

$$S_{11} = \frac{(h_{11} - Z_{01}^*)(1 + h_{22}Z_{02}) - h_{12}h_{21}Z_{02}}{(Z_{01} + h_{11})(1 + h_{22}Z_{02}) - h_{12}h_{21}Z_{02}} \qquad S_{21} = \frac{-2h_{21}\sqrt{R_{01}R_{02}}}{(Z_{01} + h_{11})(1 + h_{22}Z_{02}) - h_{12}h_{21}Z_{02}}$$

$$S_{12}=\frac{2h_{12}\sqrt{R_{01}R_{02}}}{(Z_{01}+h_{11})(1+h_{22}Z_{02})-h_{12}h_{21}Z_{02}}$$

$$S_{22}=\frac{(Z_{01}+h_{11})(1-h_{22}Z_{02}^{*})+h_{12}h_{21}Z_{02}^{*}}{(Z_{01}+h_{11})(1+h_{22}Z_{02})-h_{12}h_{21}Z_{02}}$$

S-Parameters from ABCD-Parameters

$$S_{11}=\frac{AZ_{02}+B-CZ_{01}^{*}Z_{02}-DZ_{01}^{*}}{AZ_{02}+B+CZ_{01}Z_{02}+DZ_{01}}$$

$$S_{11}=\frac{2\sqrt{R_{01}R_{02}}}{AZ_{02}+B+CZ_{01}Z_{02}+DZ_{01}}$$

$$S_{11}=\frac{2(AD-BC)\sqrt{R_{01}R_{02}}}{AZ_{02}+B+CZ_{01}Z_{02}+DZ_{01}\sqrt{}}$$

$$S_{11}=\frac{-AZ_{02}^{*}+B-CZ_{01}Z_{02}^{*}+DZ_{01}}{AZ_{02}+B+CZ_{01}Z_{02}+DZ_{01}}$$

T-Parameters from Z-Parameters

$$T_{11}=\frac{(Z_{11}+Z_{01})(Z_{22}+Z_{02})-Z_{12}Z_{21}}{2Z_{21}\sqrt{R_{01}R_{02}}\sqrt{}}$$

$$T_{21}=\frac{(Z_{11}-Z_{01}^{*})(Z_{22}+Z_{02})-Z_{12}Z_{21}}{2Z_{21}\sqrt{R_{01}R_{02}}\sqrt{}}$$

$$T_{12}=\frac{(Z_{11}+Z_{01})(Z_{02}^{*}-Z_{22})+Z_{12}Z_{21}}{2Z_{21}\sqrt{R_{01}R_{02}}\sqrt{}}$$

$$T_{21}=\frac{(Z_{01}^{*}-Z_{11})(Z_{22}-Z_{02}^{*})+Z_{12}Z_{21}}{2Z_{21}\sqrt{R_{01}R_{02}}\sqrt{}}$$

T-Parameters from Y-Parameters

$$T_{11}=\frac{(-1-Y_{11}Z_{01})(1+Y_{22}Z_{02})+Y_{12}Y_{21}Z_{01}Z_{02}}{2Y_{21}\sqrt{R_{01}R_{02}}}$$

$$T_{21}=\frac{(Y_{11}Z_{01}^{*}-1)(1+Y_{22}Z_{02})-Y_{12}Y_{21}Z_{01}^{*}Z_{02}}{2Y_{21}\sqrt{R_{01}R_{02}}}$$

$$T_{12}=\frac{(1+Y_{11}Z_{01})(1-Y_{22}Z_{02}^{*})+Y_{12}Y_{21}Z_{01}Z_{02}^{*}}{2Y_{21}\sqrt{R_{01}R_{02}}}$$

$$T_{22}=\frac{(1-Y_{11}Z_{01}^{*})(1-Y_{22}Z_{02}^{*})+Y_{12}Y_{21}Z_{01}^{*}Z_{02}^{*}}{2Y_{21}\sqrt{R_{01}R_{02}}}$$

T-Parameters from h-Parameters

$$T_{11}=\frac{(-h_{11}-Z_{01})(1+h_{22}Z_{02})+h_{12}h_{21}Z_{02}}{2h_{21}\sqrt{R_{01}R_{02}}}$$

$$T_{21}=\frac{(Z_{01}^{*}-h_{11})(1+h_{22}Z_{02})+h_{12}h_{21}Z_{02}}{2h_{21}\sqrt{R_{01}R_{02}}}$$

$$T_{12}=\frac{(h_{11}+Z_{01})(1-h_{22}Z_{02}^{*})+h_{12}h_{21}Z_{02}^{*}}{2h_{21}\sqrt{R_{01}R_{02}}}$$

$$T_{22}=\frac{(h_{11}-Z_{01}^{*})(1-h_{22}Z_{02}^{*})+h_{12}h_{21}Z_{02}^{*}}{2h_{21}\sqrt{R_{01}R_{02}}}$$

T-Parameters from ABCD-Parameters

$$T_{11}=\frac{AZ_{02}+B+CZ_{01}Z_{02}+DZ_{01}}{2\sqrt{R_{01}R_{02}}}$$

$$T_{21}=\frac{AZ_{02}+B+CZ_{01}^{*}Z_{02}-DZ_{01}^{*}}{2\sqrt{R_{01}R_{02}}}$$

$$T_{12}=\frac{AZ_{02}^{*}-B+CZ_{01}Z_{02}^{*}-DZ_{01}}{2\sqrt{R_{01}R_{02}}}$$

$$T_{22}=\frac{AZ_{02}^{*}-B-CZ_{01}^{*}Z_{02}^{*}+DZ_{01}^{*}}{2\sqrt{R_{01}R_{02}}}$$

Y-Parameters from Z-Parameters

$$Y_{11}=\frac{Z_{02}^{*}(T_{11}-T_{21})-Z_{02}(T_{12}-T_{22})}{T_{11}Z_{01}^{*}Z_{02}^{*}-T_{12}Z_{01}^{*}Z_{02}+T_{21}Z_{01}Z_{02}^{*}-T_{22}}$$

$$Y_{21}=\frac{-2\sqrt{R_{01}R_{02}}}{T_{11}Z_{01}^{*}Z_{02}^{*}-T_{12}Z_{01}^{*}Z_{02}+T_{21}Z_{01}Z_{02}^{*}-T_{22}}$$

$$Y_{12}=\frac{-2\sqrt{R_{01}R_{02}}\left(T_{11}T_{22}-T_{12}T_{21}\right)}{T_{11}Z_{01}^{*}Z_{02}^{*}-T_{12}Z_{01}^{*}Z_{02}+T_{21}Z_{01}Z_{02}^{*}-T_{22}}$$

$$Y_{22}=\frac{Z_{01}^{*}\left(T_{11}+T_{12}\right)+Z_{01}\left(T_{21}+T_{22}\right)}{T_{11}Z_{01}^{*}Z_{02}^{*}-T_{12}Z_{01}^{*}Z_{02}+T_{21}Z_{01}Z_{02}^{*}-T_{22}}$$

Y-Parameters from S-Parameters

$$Y_{11}=\frac{\left(1-S_{11}\right)\left(Z_{02}^{*}+S_{22}Z_{02}\right)+S_{12}S_{21}Z_{02}}{\left(Z_{01}^{*}+S_{11}Z_{01}\right)\left(Z_{02}^{*}+S_{22}Z_{02}\right)-S_{12}S_{21}Z_{01}}$$

$$Y_{21}=\frac{-2S_{21}\sqrt{R_{01}R_{02}}}{\left(Z_{01}^{*}+S_{11}Z_{01}\right)\left(Z_{02}^{*}+S_{22}Z_{02}\right)-S_{12}S_{21}Z_{01}}$$

$$Y_{12}=\frac{-2S_{12}\sqrt{R_{01}R_{02}}}{\left(Z_{01}^{*}+S_{11}Z_{01}\right)\left(Z_{02}^{*}+S_{22}Z_{02}\right)-S_{12}S_{21}Z_{01}}$$

$$Y_{22}=\frac{\left(Z_{01}^{*}+S_{11}Z_{01}\right)\left(1-S_{22}\right)+S_{12}S_{21}Z_{01}}{\left(Z_{01}^{*}+S_{11}Z_{01}\right)\left(Z_{02}^{*}+S_{22}Z_{02}\right)-S_{12}S_{21}Z_{01}}$$

Z-Parameters from T-Parameters

$$Z_{11}=\frac{Z_{01}^{*}\left(T_{11}+T_{12}\right)+Z_{01}\left(T_{21}+T_{22}\right)}{T_{11}+T_{12}-T_{21}-T_{22}}$$

$$Z_{21}=\frac{2\sqrt{R_{01}R_{02}}}{T_{11}+T_{12}-T_{21}-T_{22}}$$

$$Z_{12}=\frac{2\sqrt{R_{01}R_{02}}\left(T_{11}T_{22}-T_{12}T_{21}\right)}{T_{11}+T_{12}-T_{21}-T_{22}}$$

$$Z_{11}=\frac{Z_{02}^{*}\left(T_{11}-T_{21}\right)-Z_{02}\left(T_{12}+T_{22}\right)}{T_{11}+T_{12}-T_{21}-T_{22}}$$

h-Parameters from S-Parameters

$$h_{11}=\frac{\left(Z_{01}^{*}+S_{11}Z_{01}\right)\left(Z_{02}^{*}+S_{22}Z_{02}\right)-S_{12}S_{21}Z_{01}}{\left(1-S_{11}\right)\left(Z_{02}^{*}+S_{22}Z_{02}\right)+S_{12}S_{21}Z_{02}}$$

$$h_{21}=\frac{-2S_{21}\sqrt{R_{01}R_{02}}}{\left(1-S_{11}\right)\left(Z_{02}^{*}+S_{22}Z_{02}\right)+S_{12}S_{21}Z_{02}}$$

$$h_{12}=\frac{2S_{12}\sqrt{R_{01}R_{02}}}{\left(1-S_{11}\right)\left(Z_{02}^{*}+S_{22}Z_{02}\right)+S_{12}S_{21}Z_{02}}$$

$$h_{22}=\frac{\left(1-S_{11}\right)\left(1-S_{22}\right)-S_{12}S_{21}}{\left(1-S_{11}\right)\left(Z_{02}^{*}+S_{22}Z_{02}\right)+S_{12}S_{21}Z_{02}}$$

h-Parameters from T-Parameters

$$h_{11}=\frac{Z_{02}^{*}\left(T_{11}Z_{01}^{*}+T_{21}Z_{01}\right)-Z_{02}\left(T_{12}Z_{01}^{*}+T_{22}Z_{02}\right)}{Z_{02}^{*}\left(T_{11}-T_{21}\right)-Z_{02}\left(T_{12}+T_{22}\right)}$$

$$h_{21}=\frac{-2\sqrt{R_{01}R_{02}}}{Z_{02}^{*}\left(T_{11}-T_{21}\right)-Z_{02}\left(T_{12}+T_{22}\right)}$$

$$h_{12}=\frac{2\sqrt{R_{01}R_{02}}\left(T_{11}T_{22}-T_{12}T_{21}\right)}{Z_{02}^{*}\left(T_{11}-T_{21}\right)-Z_{02}\left(T_{12}+T_{22}\right)}$$

$$h_{22}=\frac{T_{11}+T_{12}-T_{21}-T_{22}}{Z_{02}^{*}\left(T_{11}-T_{21}\right)-Z_{02}\left(T_{12}+T_{22}\right)}$$

ABCD-Parameters from S-Parameters

$$A=\frac{\left(Z_{01}^{*}+S_{11}Z_{01}\right)\left(1-S_{22}\right)+S_{12}S_{21}Z_{01}}{2S_{21}\sqrt{R_{01}R_{02}}}$$

$$C=\frac{\left(1-S_{11}\right)\left(1-S_{22}\right)-S_{12}S_{21}}{2S_{21}\sqrt{R_{01}R_{02}}}$$

$$B=\frac{\left(Z_{01}^{*}+S_{11}Z_{01}\right)\left(Z_{02}^{*}+S_{22}Z_{02}\right)-S_{12}S_{21}Z_{01}Z_{02}}{2S_{21}\sqrt{R_{01}R_{02}}}$$

$$D=\frac{\left(1-S_{11}\right)\left(Z_{02}^{*}+S_{22}Z_{02}\right)+S_{12}S_{21}Z_{02}}{2S_{21}\sqrt{R_{01}R_{02}}}$$

ABCD-Parameters from T-Parameters

$$A=\frac{Z_{01}^{*}\left(T_{11}+T_{12}\right)+Z_{01}\left(T_{21}+T_{22}\right)}{2\sqrt{R_{01}R_{02}}}$$

$$C=\frac{T_{11}+T_{12}-T_{21}-T_{22}}{2\sqrt{R_{01}R_{02}}}$$

$$B = \frac{Z_{02}^{*}\left(T_{11}Z_{01}^{*} + T_{21}Z_{01}\right) - Z_{02}\left(T_{21}Z_{01}^{*} + T_{22}Z\right)}{2\sqrt{R_{01}R_{02}}} \qquad D = \frac{Z_{02}^{*}\left(T_{11} - T_{21}\right) - Z_{02}\left(T_{12} - T_{22}\right)}{2\sqrt{R_{01}R_{02}}}$$

A.2 COMSOL Settings and verification

In order to verify the validation of the voltage method and the current method, we simulate a model as depicted in following figure.

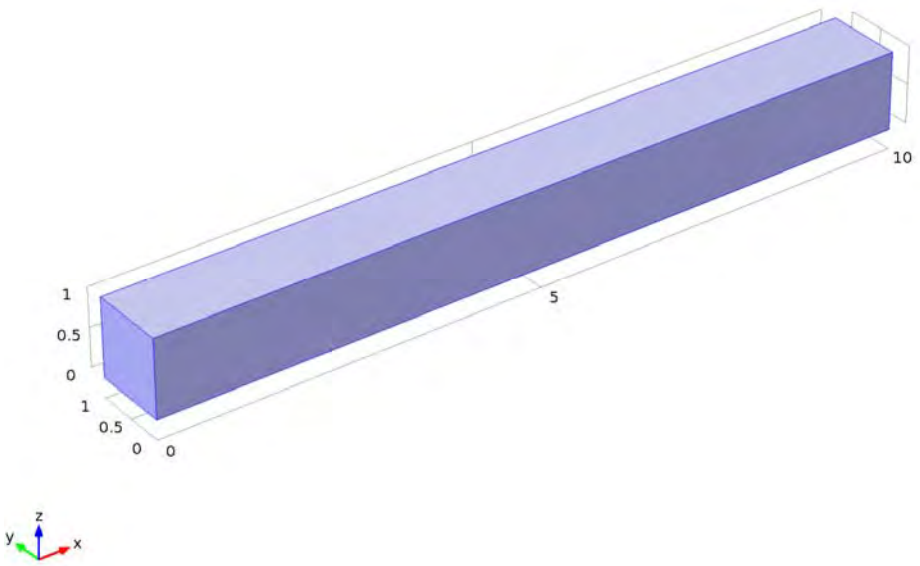


Figure A- 1 An example model in COMSOL

The dimension is 10μm, 1μm and 1μm in x,y and z direction respectively. The simulation frequency is 50Hz.

For material physic property, we set 10S/m for conductivity and 10 as the relative permittivity. So, in low frequency (e.g. 50Hz), we should have the result as,

$$R = \frac{l}{\sigma S} = \frac{lx}{\sigma \cdot ly \cdot lz} = \frac{10\mu m}{10S/m \times 1\mu m \times 1\mu m} = 1e6(\Omega)$$

$$C = \frac{\varepsilon S}{d} = \frac{\varepsilon \cdot ly \cdot lz}{lx} = \frac{10\varepsilon_0 \times 1\mu m \times 1\mu m}{10\mu m} = 1e-6\varepsilon_0 \approx 8.8542e-18(F)$$

A.2.1 Voltage Method in COMSOL

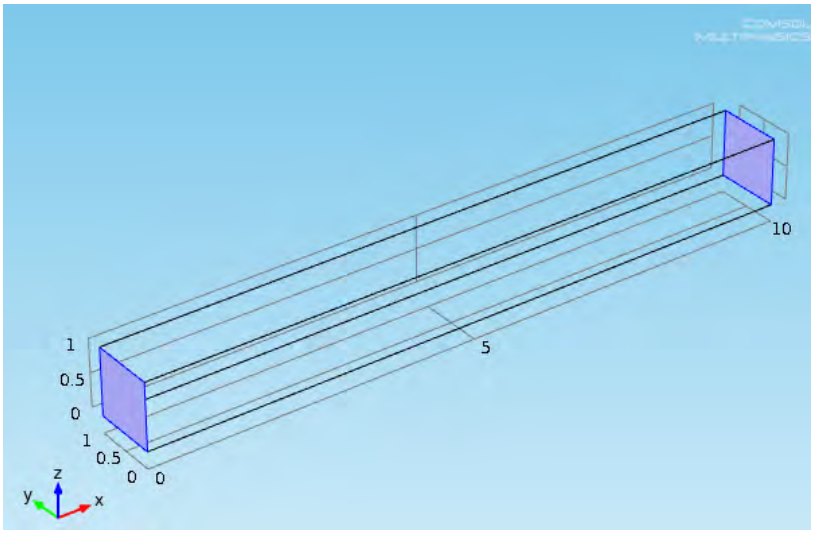


Figure 6-1 Ports of the example model

The port settings are shown in above figure, the left was set Terminal 1 and the right one is Terminal 2. All the other boundaries are set as electrical insulation.

We set the voltage of Terminal 1 as 1V and Terminal 2 as 0V as follows.

Terminal name	Terminal type	Electrical potential(V)
1	Voltage	1
2	Voltage	0

The results are as follows,

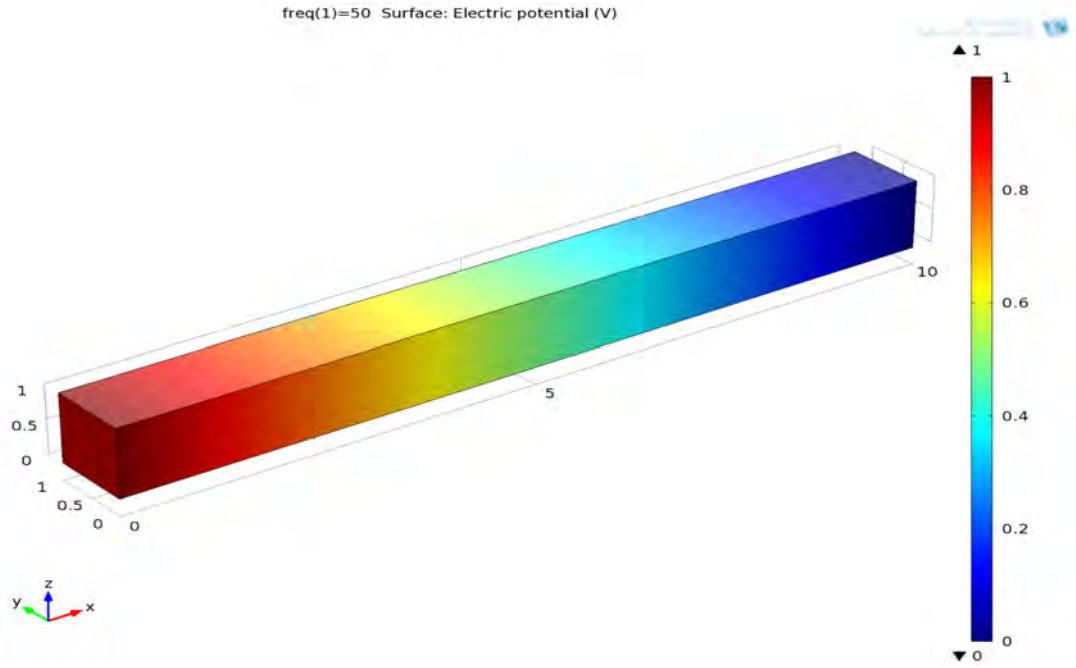


Figure 6-2 Electrical potential distribution

Table A-6-1 Capacitance calculated under different frequency

Freq(Hz)	Admittance (S)	C=imag(ec.Y21)/freq/pi/2 (F)
50.0	-1.0000000735E-6-2.781625E-15i	-8.854188467406989E-18
500.0	-1.0000000735E-6-2.7816253E-14i	-8.854188467406989E-18

So, the resistance is real(1/Y)=1e6(ohm).

From above table and figure we can see the voltage method simulation results are **accurate**.

A.2.2 Current Method in COMSOL

The current method is to inject 1A current to a terminal and -1A for the other one. Then we calculate the voltage on every terminal to get the impedance.

A “ground” boundary condition should be set.

a) No isolated layer

Because we need a ground surface, so we set bottom surface of model as “ground” boundary condition without adding any isolated layer.

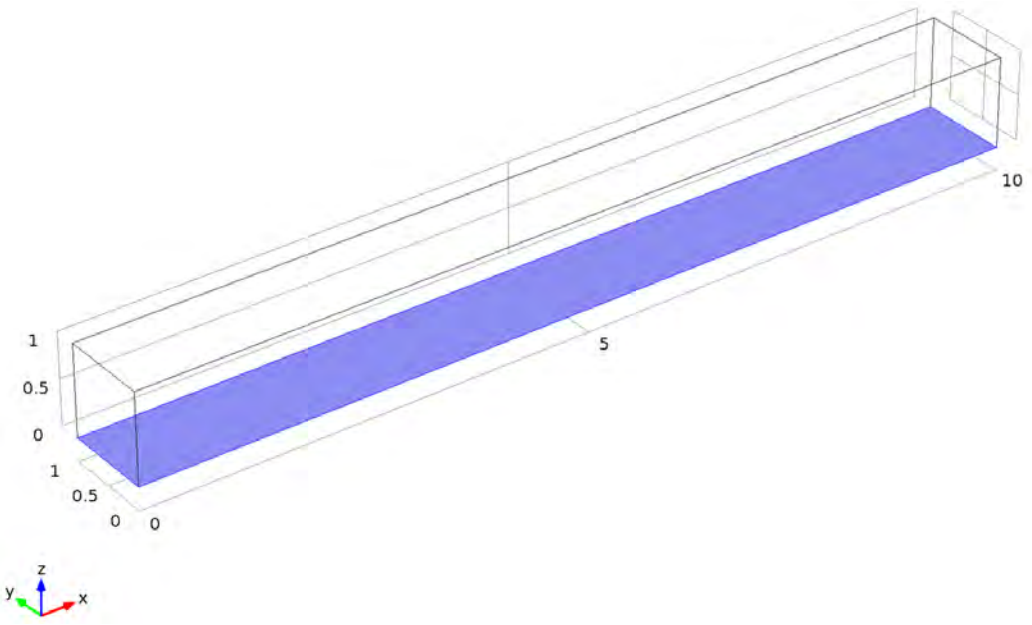


Figure 6-3 Set bottom surface of model as “ground” boundary condition

The result is,

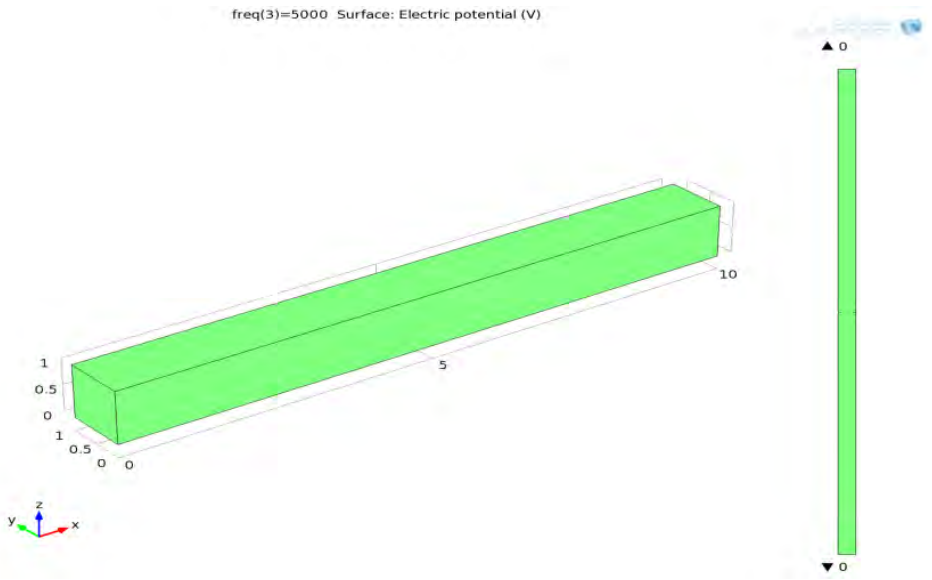


Figure 6-4 Surface electric potential without isolated layer

That's means we cannot set ground surface like this. It's not correct result.

b) Add isolated layer

Due to above simulation, we should add a new isolated layer under our model as shown in following figure. We set its conductivity as 0S/m and relative permittivity as 1.

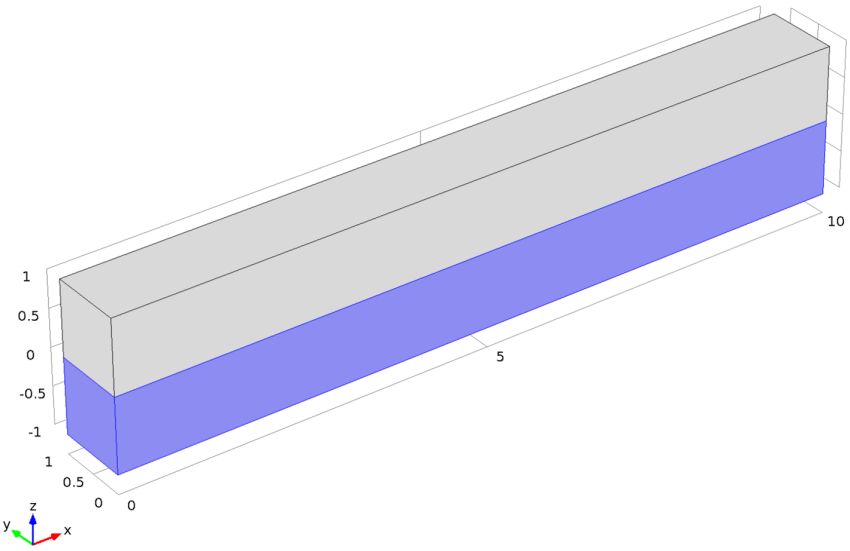


Figure 6-5 Add the isolated layer

We set the ground condition as follows.

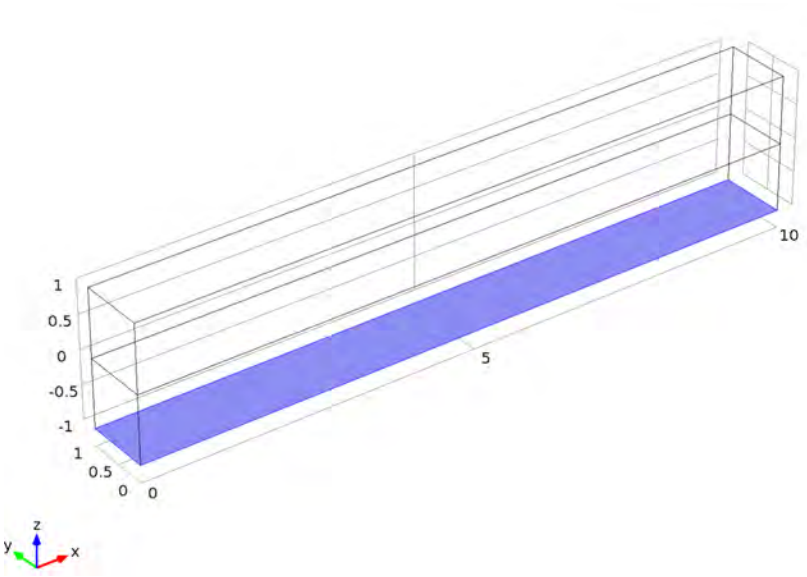


Figure 6-6 Set “ground” boundary condition

The terminals location are the same as in voltage method (in the left end and right end of the upper layer) and property are shown in table following.

Terminal name	Terminal type	Terminal current(A)
1	**Current**	**1**
2	**Current**	**-1**

The results are as follows,

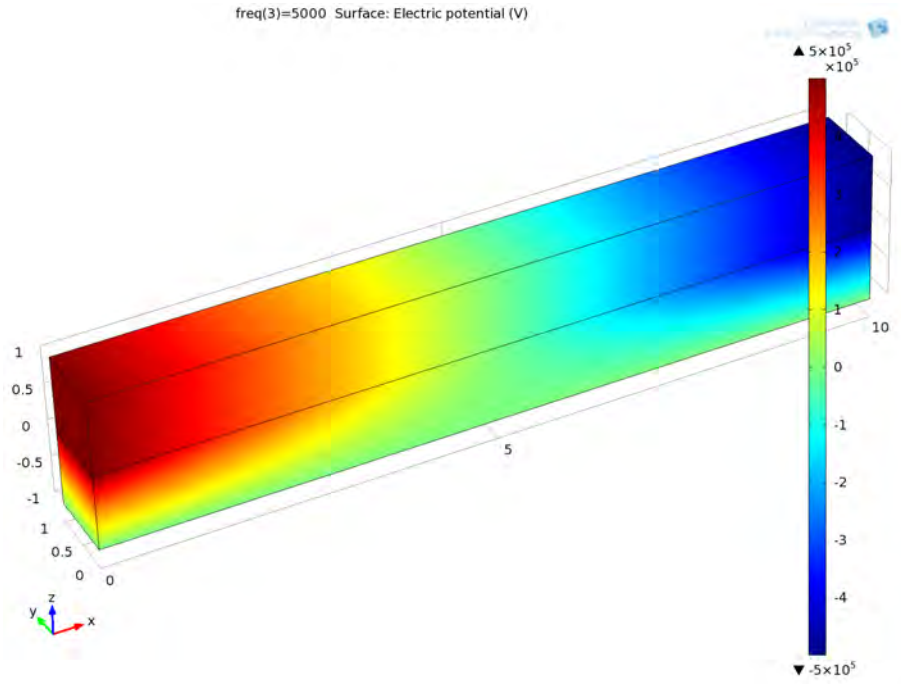


Figure 6-7 Surface electric potential with isolated layer

Freq(Hz)	ec.V0_1-ec.V0_2 /ec.I0_1(Ω)
50.0	999999.9580480172-0.005183596893361675i
500.0	999999.9580480176-0.005183596893362119i

From above table, we can see, the resistance results are correct.

But the capacitance result is not correct as depicted following,

Freq(Hz)	(1/(imag((ec.V0_1-ec.V0_2)/ec.I0_1)))/freq/pi/2 (F)
50	-0.6140714502538407
500	-0.06140714502537881
5000	-0.006140714502537487

So, despite the resistance result is correct, the capacitance result is not correct, either.

c) No isolated layer but with ground point

If there is no isolated layer, we could also calculate right by set a point as ground instead of a surface.

We add a new point in middle of the background surface and set it as ground limited condition. (Figure following)

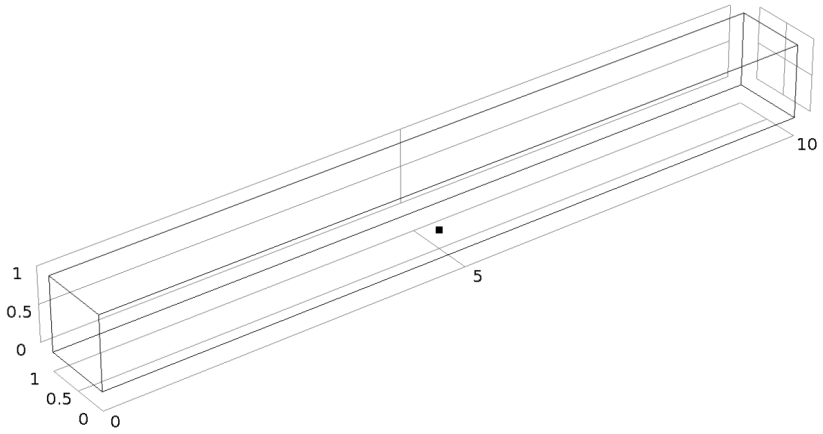


Figure 6-8 Set a point as “ground”

The result is,

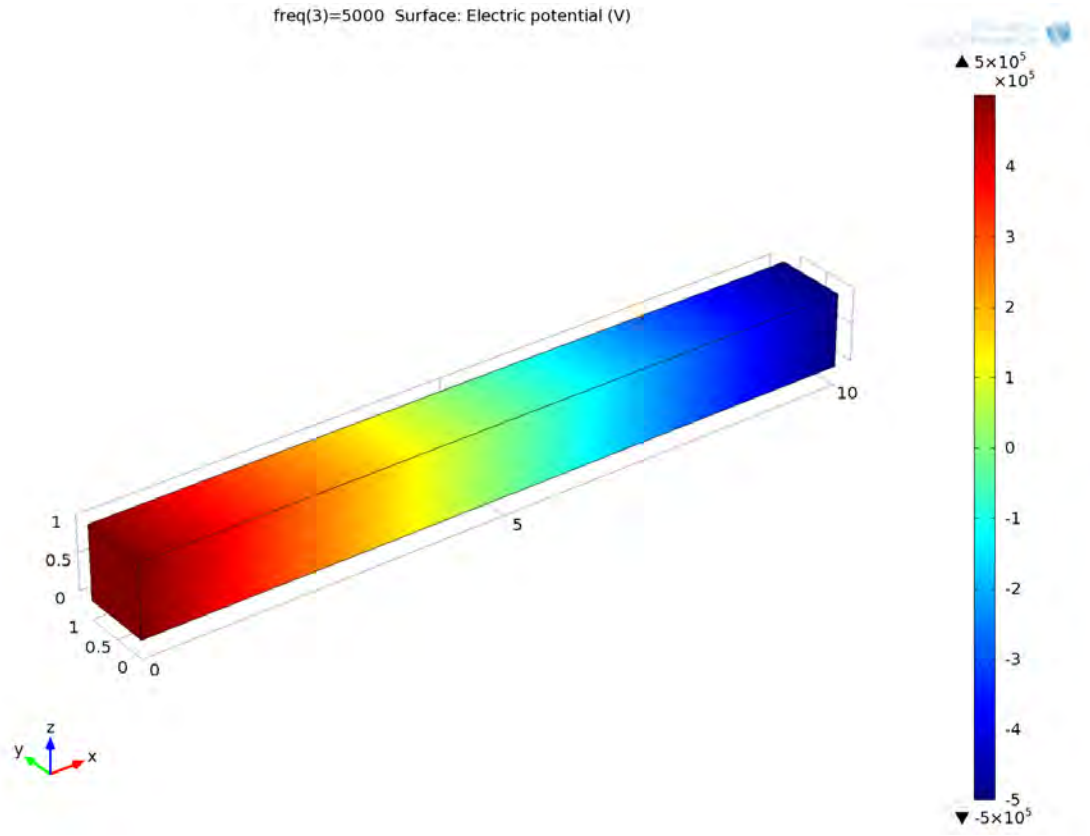


Figure 6-9 potential distribution with set of point “ground”

The impedance,

Freq(Hz)	(ec.V0_1-ec.V0_2)/ec.I0_1 (Ω)
50	10e5-0.0028i
500	10e5-0.0028i

The capacitance,

Freq(Hz)	imag(ec.I0_1/(ec.V0_1-ec.V0_2)/freq/pi/2) (F)
50	8.8542e-18
500	8.8542e-19

In fact we can set a ground point anywhere which will lead to the same result.

c) Conclusion for current method

Relative to Voltage Method, a Ground is necessary for the Current Method. We can either set a surface as Ground with an isolated layer added between in the original model and the ground surface or just set a point as Ground.

We also find the impedance is not always correct in this method for several frequencies in which the C result is not always right. But use the **Current Method** to **single** frequency model is adapted.

A.3 Export netlist in ADS.

Once complete netlist generation, we obtain a. Sp containing the description of the netlist. This file can be exported in any CAD software that can read a SPICE netlist. Tools available, the most convenient is ADS. This section shows how to model a black box in ADS containing the description of SPICE file. Initially, it creates a "Project" in ADS containing several directories that stores design, simulation results. The SPICE file 3D-TLE should be placed in the data directory (Figure 6-10).

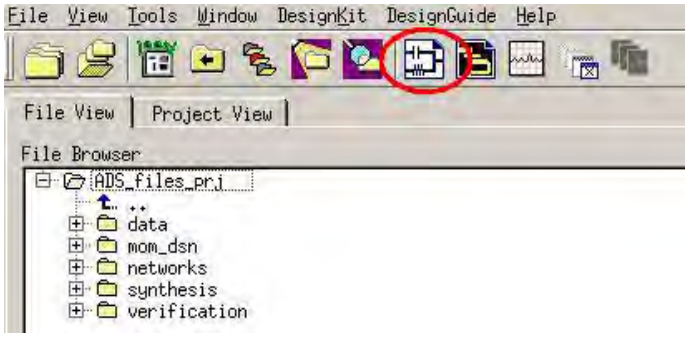


Figure 6-10: Illustration of the distribution of folders inside of a "Project" ADS (ADS_file_prj being called here). The file is stored SPICE/3DTLE/in "data".

Then we open a new schematic editing window. This can be done by clicking on the icon circled in red visible on the previous figure.

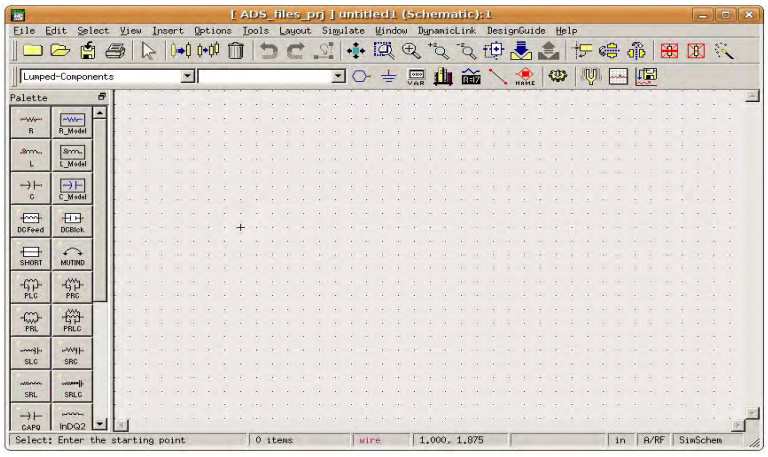


Figure 6-11: Editing window in ADS.

It then goes into the menu at the top of the window and we did: Tools → HSPICE Compatibility Wizard. A new window appears from which the. Sp file contained in "data" (Figure 6-12) is loaded. This step corresponds to step 1/6 of the creation of the black box. The second step asks you to specify the name of the black box. By default, the name chosen by ADS is the name of the file. Sp

Figure 6-12: Window to load the SPICE file for the creation of the black box.

Step 3/6, much more important, select the nodes of the system described in the netlist that will serve as I/O ports in the black box. Note that you can access from this window to the description SPICE via the "View HSPICE file" tab. In Figure 6-13, was selected nodes in and out for the I/O ports of the black box.

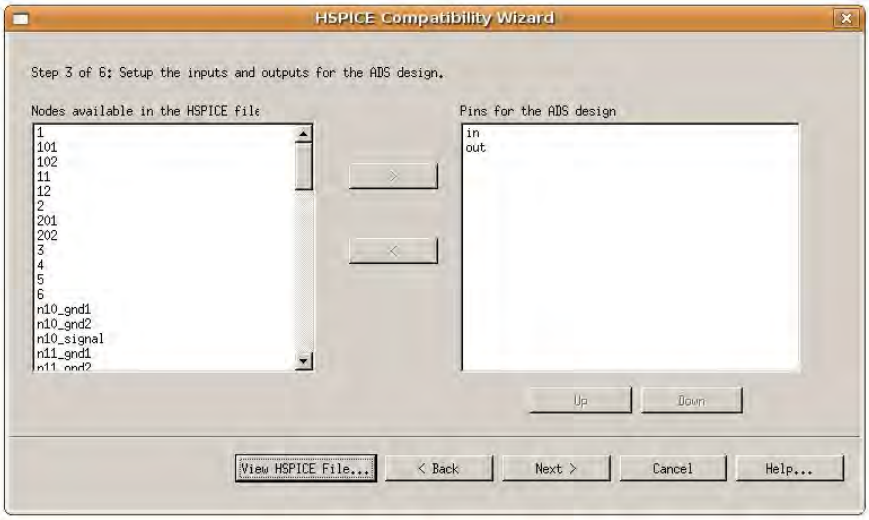


Figure 6-13: Step 3/6: selection of nodes present in the SPICE description will serve as I/O ports in the black box.

The next step is then to create the symbol of the black box. In the case of a box with two or three ports, it is not necessary to define the symbol itself. By cons, in the context of matrices, it is preferable for reasons of readability if the number of I/O ports is important. To do this, click on the "Edit Symbol Generator Setting" tab. One can define the symbol as a quadrupole manage the distance between the pins

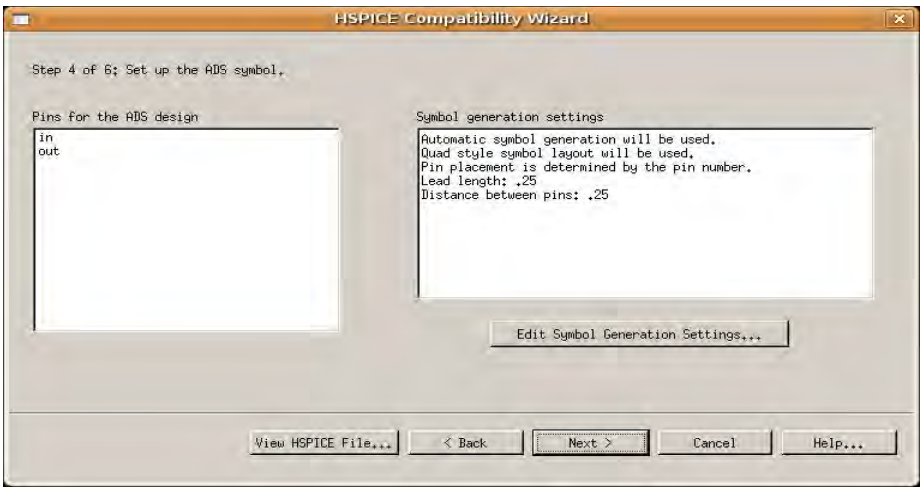


Figure 6-14: Step 4/6 edition of the symbol of the black box.

The next steps are to give values to the parameters of the netlist that have been declared as variables in a netlist, which is not the case of netlists generated by 3D-TLE and to validate the definition of the black box. Therefore, it "jumps" steps 5 and 6. Finally we get our black box as shown in Figure 6-15 and the pins which correspond to those which had been defined Figure 6-12.

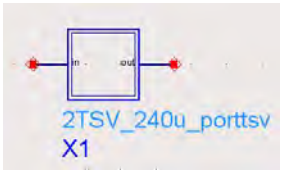


Figure 6-15: Step 4/6: Black Box SPICE/3D-TLE containing the description of a structure.

Finally, one can access the netlist through a "down hierarchical" in the black box via two options schematic menu circled in red in the following figure. Note that you can change at will the description of the netlist.

Figure 6-16: Options "to go up or down" hierarchically in a black box ads.

Note: if the data in fichier.sp is replaced by a file with the same name, the netlist is changed automatically sees. However, to ensure that the netlist matches the modified file, it may be preferable to remove the black box and recreate a schematic symbol.

Appendix B Résumé en français

L'intégration 3D est peut-être la solution technologique la plus prometteuse pour suivre le niveau d'intégration dicté par la fameuse loi de Moore. Elle entraine des travaux de recherche importants depuis une douzaine d'années. Elle permet de superposer différents circuits et composants dans un seul boitier. Son principal avantage est de permettre une association de technologies hétérogènes et très spécialisées pour la constitution d'un système complet, tout en préservant un très haut niveau de performance grâce à des connexions très courtes entre ces différents circuits.

L'objectif premier de ce travail est de fournir des modélisations de substrats couplés avec leur connectique interne: via traversant, ou/et contacts dans le substrat… avec plusieurs degrés de finesse/précision, pour permettre au concepteur de haut niveau de gérer et surtout d'optimiser le partitionnement entre les différentes strates. Cette modélisation passera par le développement de plusieurs vues à différents niveaux d'abstraction: du modèle physique au modèle «haut niveau».

B.1 Introduction

L'industrie électronique est la plus grande industrie depuis 1996 et a atteint environ 1,5 milliards de dollars à la fin de l'année 2011 [1, 2]. La proposition de doubler le nombre de transistors sur une puce tous les 24 mois par Gordon Moore en 1965 (la soi-disante loi de Moore [3]) a été le « moteur » le plus puissant de l'importance de l'industrie de la microélectronique au cours des 50 dernières années [4]. Cette loi améliore la mise à l'échelle et l'intégration via la lithographie, en deux dimensions (2D), de toutes les fonctions sur une même puce. Les finalités de ces technologies intégrées sont des systèmes sur puce (SoC) [5] et des systèmes en boîtier (SiP) [6].

Comme conséquence de l'exigence de fréquences d'horloge plus élevées et de plus faibles consommations d'énergie, de nos jours, ces technologies planaires 2D traditionnelles commencent à faire face aux défis à partir de points de vue techniques et financiers: limites physiques, complexité du traitement, coûts de fabrication, etc. Il s'agit d'une forte augmentation du « quantitatif » et « du qualitatif » sur certains nombres de caractéristiques, nécessaires pour les multimédia actuels et futurs ou les applications mobiles ; la complexité de la conception est augmentée de façon exponentielle. Mise à l' échelle de la technologie, ainsi que l'intégration de technologies disparates dans une seule puce, signifie que la performance du dispositif continue à devancer les domaines de l'interconnexion et les capacités d'encapsulation, et donc il existe de nombreuses difficultés techniques, notamment en matière de gestion d'énergie, dissipation thermique au niveau intra et intercommunications de la puce. » [7] Les retards dans les lignes d'interconnexion deviennent aussi un obstacle dans les systèmes 2D à très grande intégration (cf. ULSI) par rapport à la dissipation de puissance, les délais dans les transistors, etc. Par conséquent, les approches technologiques autres que d'échelle sont maintenant investiguées en vue de suivre ou d'obtenir plus que la loi de Moore.

La nouvelle technologie d'intégration en trois dimensions (3D) avec de plus petits facteurs de forme, la densité d'intégration plus élevée et la volonté de réaliser des puces à technologie mixte, semble être le candidat le plus prometteur. [8]-[9] Il est considéré comme un moyen efficace pour améliorer les performances [10] par rapport aux schémas classiques en 2D ; les avantages potentiels de l'intégration 3D sont nombreux, comme l'amélioration des performances et de combinaisons de systèmes hétérogènes flexibles (logique CMOS, fonction analogique RF, mémoires). Les empilement ICs verticaux permettent le raccourcissement significatif des réseaux de lignes d'interconnexion (Figure B-1), diminuant ainsi les retards de

ligne d'interconnexion, qui deviennent un obstacle majeur dans les systèmes V(U)LSI 2D par rapport aux retards de commutation des transistors, la dissipation d'énergie tout en augmentant la densité d'intégration, menant à de plus petits facteurs de forme et une réduction des coûts de fabrication [11, 12].

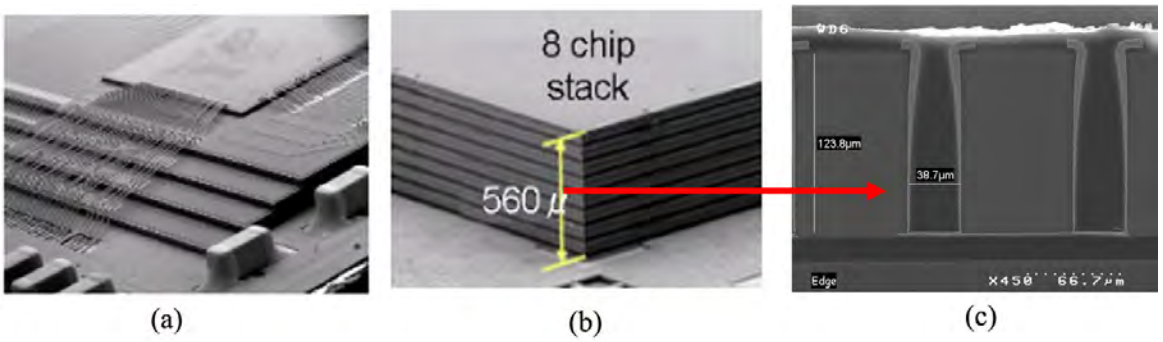


Figure B-1 (a) Puces empilées avec « wire bonding ». (b) 3D TSV : structure à empilement (Source: SAMSUNG). (c) Vue en coupe transversale de la structure 3D d'empilage TSV. (Source: CEA-LETI)

Actuellement, grâce au contrôle des micro et nano technologies, les systèmes intégrés 3D peuvent être obtenus par l'empilement de circuits intégrés 2D verticalement à l'aide de « wire-bonding ». (Figure B-2) Mais le wire-bonding ne permet pas la connexion des plots d'entrée / sortie puce situés à leur périmètre. En outre, le wire-bonding présente des inconvénients en termes de retards en surface et de propagation en fonction de la fréquence de l'horloge et les longueurs de fil (Figure B-1 (a)). En conséquence, les nouvelles technologies d'intégration 3D semblent nécessaires. D'une manière générale, l'intégration 3D se compose de : 3D IC packaging, intégration 3D IC, et l'intégration 3D Si [4] [13].

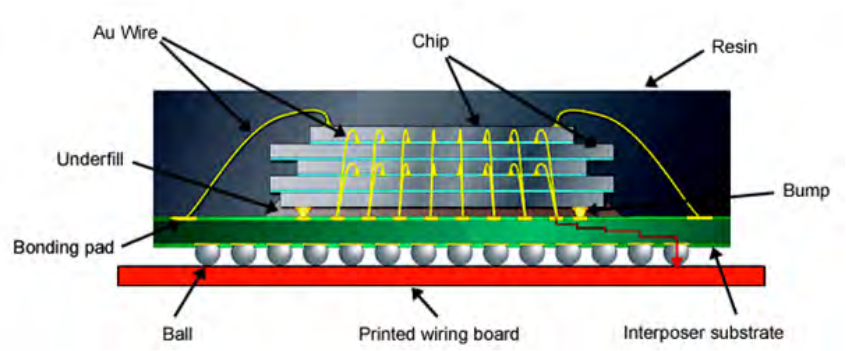


Figure B-2 Exemple de structure SiP (technologie SIP de 5 puces empilées) (Source: Renesas[14])

La technologie 3D est confrontée à de nombreux défis technologiques, comme la réalisation d'interconnexions verticales qui assurent la transmission du signal, la liaison avec l'alignement des filières fonctionnelles et le substrat amincis.

Les via silicium traversant (TSV) viennent à point et rendent les circuits 3D davantage réalisables. En fait, William Shockley avait « intuité » les TSVs il ya plus de 50 ans [15, 16], mais il n'a pas été prévu pour la 3D Si / IC intégration à ce moment-là. Maintenant, il joue un rôle important dans cette technologie ; il sépare le « packaging » 3D IC de 3D IC / Si intégration, alors que les deux derniers utilisent des TSVs, mais pas le packaging 3D IC. Il existe également des différences entre 3D IC et 3D Si. intégrations [17] ; 3D IC intégration empile des puces avec des billes(bumps) tandis que 3D Si intégration empile des tranches sans ces billes [18].

Un exemple d'empilement TSV 3D avec trois circuits est montré à la Figure B-3. Les connexions électriques sont assurées par de nouvelles structures pré ou post-traitement: les

couches métalliques de redistribution (RDL), piliers de cuivre et TSVs. Les lignes de redistribution arrière et une densité différente de TSVs permettent la construction de structures d'interconnexion 3D, denses et complexes du point de vue mécanique et électrique reliant les différents circuits classiques empilés. La RDL est utilisée pour distribuer l'énergie et les signaux à haute vitesse sur les surfaces supérieure ou inférieure d'une filière et les TSVs est une technologie clé pour l'intégration 3D, propageant des signaux à travers des couches de silicium dans les systèmes. Des billes de soudure sont mises à l'arrière des couches des systèmes 3D pour assurer la liaison avec leur environnement.

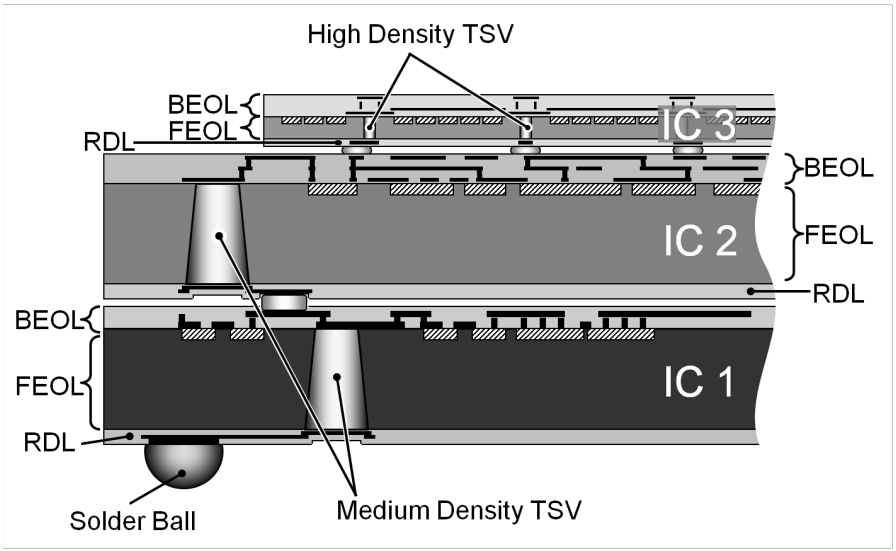


Figure B-3 Exemple d'un empilement vertical/3-D, avec trois ICs

L'intégration 3D permet aussi l'intégration de différents types de puces et les dispositifs dans un « paquet » unique Figure B-4), ou un sous-système compact offrant un maximum de profit de technologies hautement spécialisées et hétérogènes. Toutefois, afin de profiter pleinement de la « 3D IC », la décision doit venir en amont dans le processus de planification de l'architecture plutôt que comme une décision du packaging après que la conception circuit soit finalisée. [19] Cela exige de prendre en l'espace de conception 3D, dès le début de la conception du système, en vue de distribuer ses différentes parties fortement intriquées.

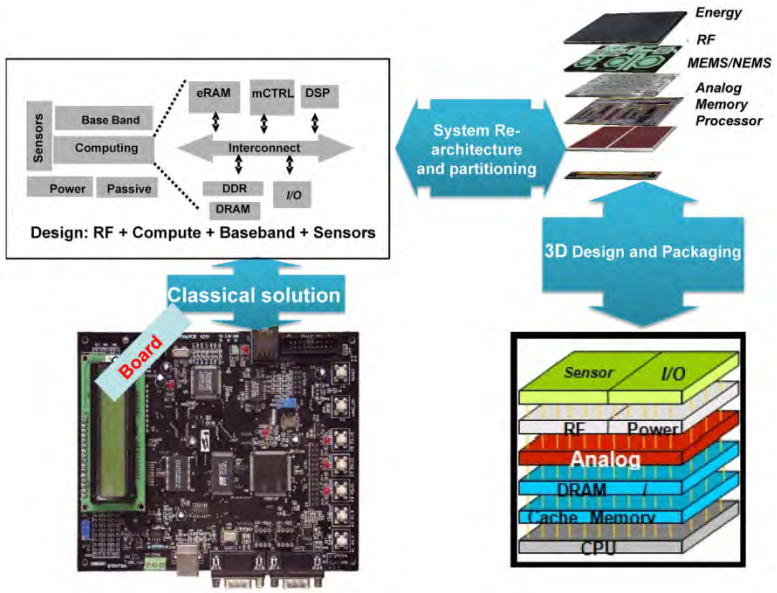


Figure B-4 Solution 2D classique contre le concept 3D

Le dispositif TSV 3D donne un moyen clair de développement de l'industrie électronique. Des prévisions réalistes sont de 7 à 16 millions de plaquettes «3D TSV» pour 2016 [20]. Ces circuits intégrés 3D, où les interconnexions sont prises au niveau global ou partiel dans la puce , permettent une meilleure intégration, une grande bande passante et des performances électriques en réduisant les délais de signaux ,avec un plus petit facteur de forme et le nombre de broches réduit, et globalement une meilleure compacité. Dans ce type de technologie, les solutions les plus courantes utilisent alors des dispositifs de mémoire empilés [21-24], mais également des capteurs, notamment CMOS (imagerie) [25-29] accolés avec des DSPs (Digital Signal Processing). Les applications futures visent à empaqueter les processeurs multi-noyaux, les mémoires caches hiérarchisées et d'autres technologies incompatibles dans les solutions actuelles d'intégration hétérogène. La Figure B-5 montre une feuille de route de la 3D-IC/ TSV.

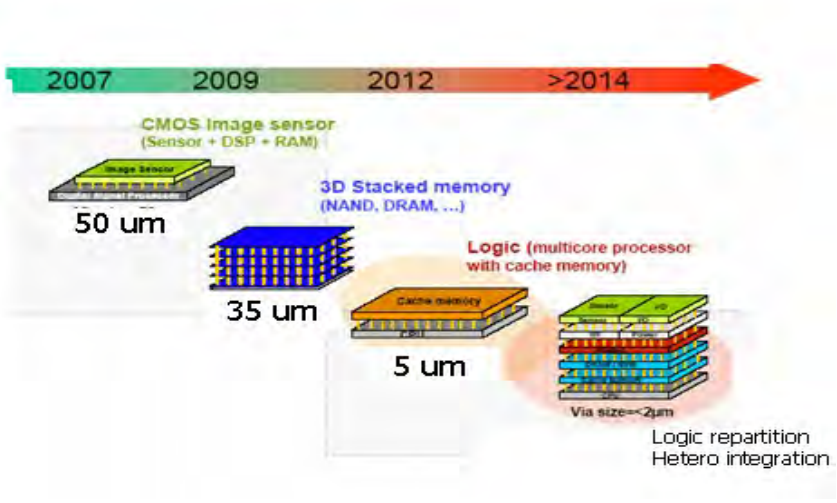
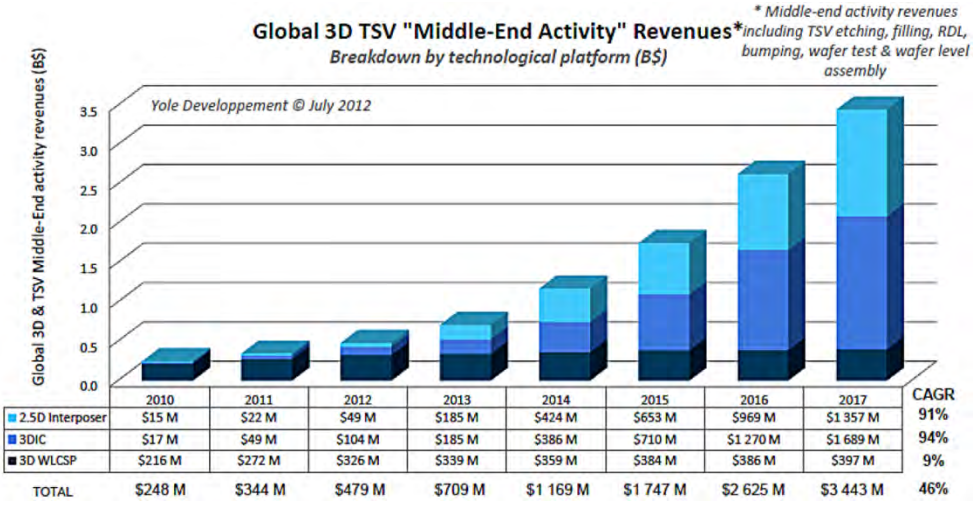


Figure B-5 Tendance de l'intégration 3D (STMicroelectronics/LETI)

Selon le rapport de Yole Développement (Figure B-6), le marché « TSV 3D « atteindra la valeur du 38 milliards de dollars en 2017 (9% du total des produits semi-conducteurs), plus de 10 fois plus rapide que l'industrie des semi-conducteurs. [30]



	2010	2011	2012	2013	2014	2015	2016	2017	CAGR
2.5D Interposer	$15 M	$22 M	$49 M	$185 M	$424 M	$653 M	$969 M	$1 357 M	91%
3DIC	$17 M	$49 M	$104 M	$185 M	$386 M	$710 M	$1 270 M	$1 689 M	94%
3D WLCSP	$216 M	$272 M	$326 M	$339 M	$359 M	$384 M	$386 M	$397 M	9%
TOTAL	$248 M	$344 M	$479 M	$709 M	$1 169 M	$1 747 M	$2 625 M	$3 443 M	46%

Figure B-6 Revenus globaux de la 3D TSV "Middle-End Activity" (Source: Yole Développement) [30]

L'application de la technologie TSV est utilisée dans des produits pratiques. En cette année (2013), le consortium de la « mémoire TSV cube » (HMC) [24] vient de publier une « HMC Spécification 1.0 ». Avec huit liens, un cube de mémoire peut atteindre un maximum

de 320 Go / bande passante totale. Cela signifie qu'il offre jusqu'à 15 fois la performance de la DDR3 (Double Data Rate 3) mémoire[31], tout en utilisant 70% d'énergie en moins.

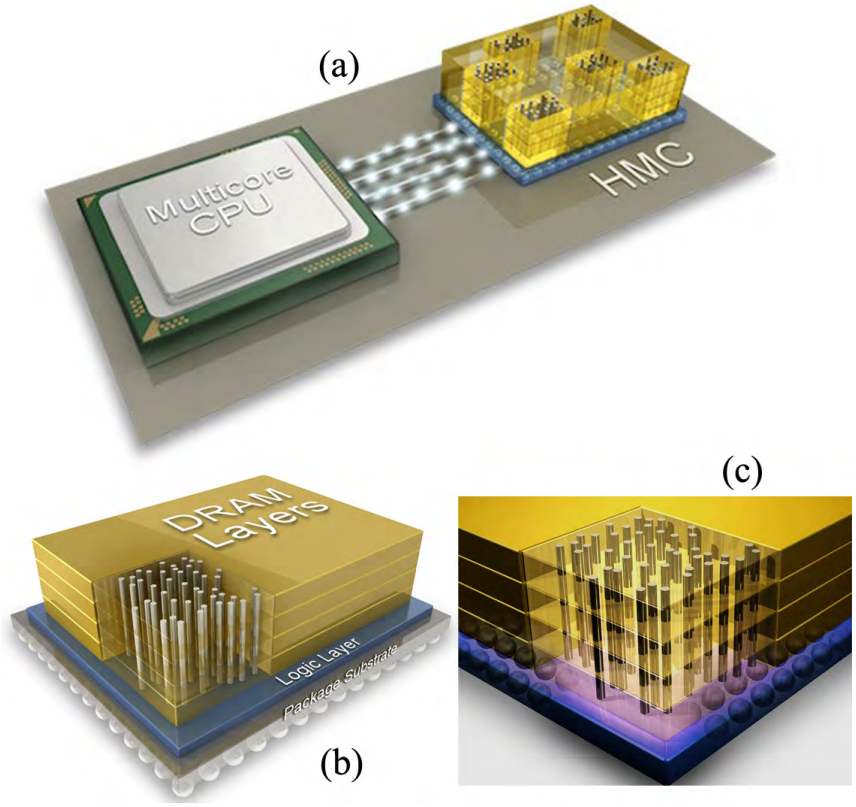


Figure B-7 Architecture de mémoire hybride mémoire cube (Source: [24])

Grâce aux apports de la technologie [21-23], la HMC est essentiellement un empilement de jusqu'à huit DRAMs (Dynamic Random Access Memory), reliées les unes aux autres par TSVs, posées au sommet de la logique qui contrôle les entrées-sorties (voir Figure B-7) Du point de vue du Consortium HMC, « Hybrid Memory Cube » est une innovation révolutionnaire dans l'architecture des mémoire sDRAM, qui établit un nouveau standard pour les performances mémoire, la consommation d'énergie et les coûts." [24] Figure B-7 (c) montre la structure du TSVs utilisé dans HMC.

Les capteurs d'image CMOS utilisant une approche "dernier via", avec des diamètres d'environ 50 microns et de semblables épaisseurs de silicium, ont déjà été introduits sur le marché[32]. La Figure B-8 montre un nouveaux processeur d'image 3-D qui utilise des TSVs pour incorporer un capteur d'image, un convertisseur A/D, la mémoire de trame, et le processeur d'image reconfigurable dans une configuration empilée à quatre couches. [33]

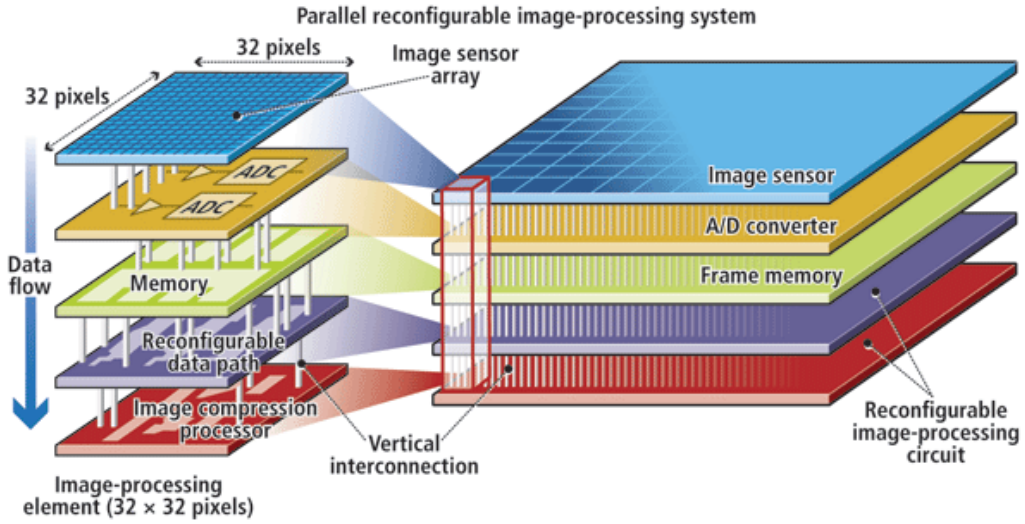


Figure B-8 Un nouveau processeur 3D d'image utilise la technologie TSV qui incorpore un capteur d'image, un convertisseur A/D, la mémoire de trame, et le processeur d'image reconfigurable, dans une configuration empilée à quatre couches. (Source: vision-systems)

Sur la Figure B-9, une prévision de produits d'intégration 3D d'ici 2017 de développement Yole est affichée [30]. De la figure, on peut voir que, d'ici 2017, les produits d'intégration 3D se trouveront, a priori, dans presque tous les domaines de l'électronique. Et le téléphone mobile va prendre 42% de tous les produits d'intégration 3D, en raison de sa demande de portabilité qui bénéficiera grandement de cette technologie.

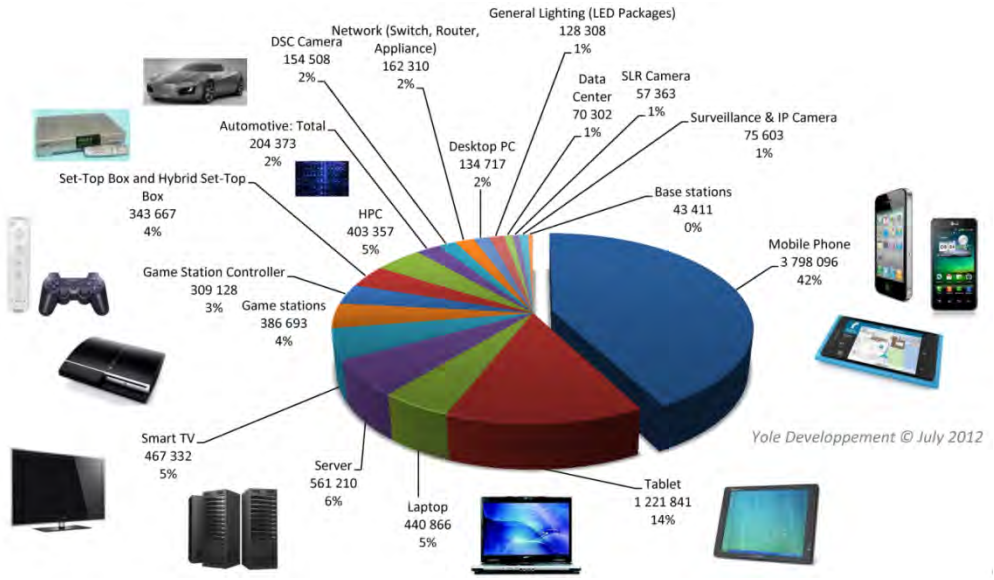


Figure B-9 Production « intégration 3D » prévisions en 2017 (toutes plateformes 3DTSV) (Source: Yole Développement)[30]

Tout d'abord, dans le chapitre 1, l'introduction donne un état de l'art du circuit intégré 3D. Nous affirmons que les architectures 3D pour l'intégration IC sont une alternative prometteuse aux conceptions 2D, quant à augmenter les densités d'interconnexions et la réduire le coût de de fabrication.

Le chapitre 2 présente quelques connaissances de base sur les ICs 3D et le bruit substrat. Le défi rencontré en 3D et les technologies de fabrication des TSVs sont également étudiés. Des méthodes classiques d'analyse de bruit de substrat de dispositifs analogiques sont introduites.

Dans le chapitre 3, nous proposons une nouvelle technique d' « extraction » d'un réseau électrique pour le substrat, en s'appuyant sur une matrice de lignes de transmission pour les circuits 3D. Le couplage du substrat et les pertes dans les circuits intégrés peuvent être analysés par ces algorithmes. Cette technique pourrait être utilisée pour les contacts métalliques et / ou TSV, quelque soit le nombre ; ils peuvent être placés « n'importe où » dans le substrat, ou au-dessus. Cette caractéristique le rend très approprié pour les substrats multicouches.

Dans le chapitre 4, des modèles compacts pour les interconnexions 3D sont extraits et un outil extracteur de ligne de transmission 3D y est développé. L'approche de modélisation est validée par des analyses en fréquence en comparant les paramètres S mesurés sur les structures de test avec ceux obtenus en simulant leurs modèles électriques équivalents respectifs sur une large gamme de fréquences, allant du continu à 20GHz.

Dans le chapitre 5, un modèle amélioré et plusieurs axes de travail futurs concernant la recherche sur la « 3-D IC » sont proposés. L'analyse d'effet (électro-)thermique, d'effet de peau et de courants de Foucault, ainsi que celle de corrélations possibles de fluctuations de sources de bruit sont également initiées.

Le chapitre 6 résume les contributions de ce travail de thèse, tire des conclusions du manuscrit.

B.2 Connaissances de base sur TSV et bruit de couplage du substrat

B.2.1. De la 2D à la 3D: Opportunités et défis

Nous avons vu que le 3D-IC a un brillant avenir. La technologie d'intégration micro-nanoélectronique 3D-**TSV** permet de superposer différents circuits et composants dans un seul boitier. Son principal avantage est de permettre une association de technologies hétérogènes et très spécialisées pour la constitution d'un système complet, tout en préservant un très haut niveau de performance grâce à des connexions très courtes entre ces différents circuits.(Figure B-10). Mais, même avec les avantages de la 3D-IC, il ya plusieurs défis majeurs à l'adoption d'architectures 3D, dus à l'intégration à haute densité et son statut de technologie émergente, notamment relier correctement caractérisation et modélisation électrique. L'intégration à haute densité et haute fréquence du système font également du bruit du couplage substrat l'une des considérations les plus importantes dans la conception, en raison de sa grande influence sur la performance des circuits intégrés[34].

Il nous faut donc des outils efficaces pour analyser la disposition pratique, pour calculer les performances électriques du circuit. Nous avons besoin de calculer les matrices résistance, capacité et 'inductance partielle, pour analyser le couplage substrat.

La méthode la plus fiable est de résoudre directement les équations de Maxwell [35], par exemple par éléments finis, avec des méthodes dans le domaine temporel aux différences finies (FDTD), etc. Ces méthodes peuvent donner des résultats très précis, une large applicabilité, mais le coût de calcul paraît rédhibitoire. Surtout avec les ordinateurs actuels : on ne peut pas résoudre les problèmes à grande échelle dans un temps acceptable. Et il est difficile d'assurer la stabilité inconditionnelle de cette méthode.

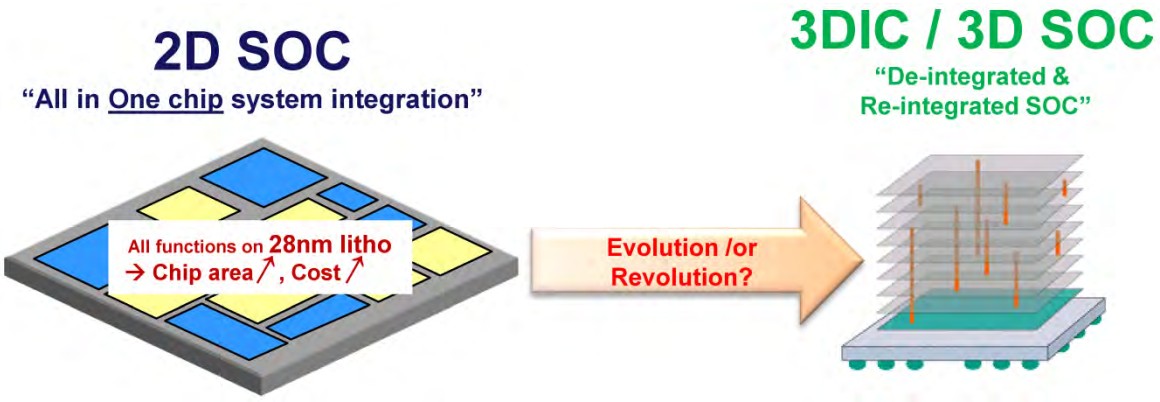


Figure B-10 2D SoC v.s. 3DIC[20]

Une première technique appelée «TSV via last» consiste, après avoir réalisé les composants actifs sur la face avant de la plaquette de silicium, à l'amincir puis à percer des trous à travers la plaque de silicium depuis la face arrière jusqu'aux métaux de la face avant. Ces trous sont alors métallisés de façon à relier les connexions de la face avant à un réseau de redistribution ajouté sur la face arrière qui permet la soudure directe sur la carte électronique (par ex. par boules de soudures). La difficulté de cette technique est d'atteindre la première couche métallique de la face avant de manière fiable, sans avoir à ouvrir des orifices trop larges, ce qui pénaliserait les dimensions de la puce. Les dimensions des trous, réalisés à partir de la, face arrière, dépendent de la technique employée et de l'épaisseur de la plaque.

Une autre technique aussi appelée ''BEOL (post Back End Of Line) via first'' peut être appliquée sur des plaques en fin de fabrication des composants actifs, mais avant amincissement des plaques. Elle consiste en la gravure et en la métallisation des TSVs sur des régions prédéfinies de la puce. Les TSV métallisés sont reliés, côté face avant, aux couches métalliques de la puce grâce à une couche de redistribution. L'amincissement de la puce dégage ensuite les TSV métallisés qui seront connectés, côté face arrière, soit directement soit par une métallisation de redistribution, à une couche métallique (type cuivre électrolytique), adaptée à un empilement avec soudure.

Les acteurs industriels les plus dynamiques sur le sujet sont: IBM[163] et Intel[164] (intégration massive de cœurs de processeurs), Samsung (intégration 3D de mémoires)[165], Tezzaron [166]. En France, les sociétés STMicroelectronics, NXP et le CEA-LETI ont lancé de nombreux programmes pour maitriser l'intégration 3D (Figure B-11 et Figure B-12). Typiquement les acteurs français travaillent sur les vias en faible densité (diamètre ~50µm, facteur de forme ~1-2) et les vias en haute densité (diamètre ~3µm, facteur de forme ~4-10). La première application est de type imageur, avec des produits déjà existants chez ST intégrant le capteur CMOS sur une puce numérique. Les premiers projets impliquant les acteurs français sont : au niveau régional *ICE3* « *ICE3* : Intégration 3D de Circuits micro Electroniques » (avec INL-INSA), au niveau national ANR *3D-IDEAS* « « *3D-IDEAS* - Technologie d'intégration et de conception 3D pour des systèmes et applications imageurs » (INL-INSA & ECL), au niveau européen Catrene *3DIM3* (INL-INSA & ECL). L'INL-INSA a pu s'insérer dans ces nouveaux projets à finalité industrielle très marquée via son expertise en intégrité du signal dans les circuits mixte (numérique et analogique).

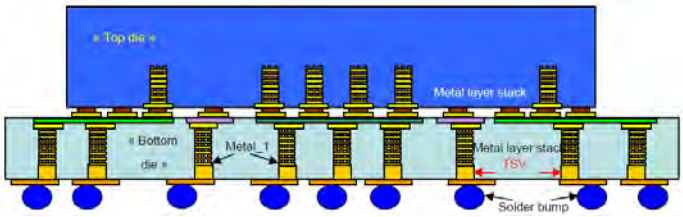


Figure B-11 Exemple d'utilisation de via traversant (dessin non à l'échelle) (STMicroelectronics/LETI)

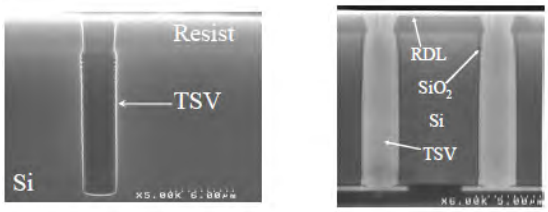


Figure B-12 **Exemple de réalisation de via traversant (LETI)**

Toujours au niveau français, le laboratoire IMEP-LAHC (site du Bourget-du-Lac) fournit une expertise en caractérisation et modélisation haute fréquence des vias traversant, de la connectique, et le positionnement complémentaire de l'INL-INSA sur la caractérisation / modélisation du via traversant, de la connectique vis-à-vis du substrat (couplage entre via et composant actifs, circuits…) semble très pertinente. Nous associons, d'ailleurs, les compétences du LAHC et de l'INL dans deux programmes engagés (régional *ICE3* et national ANR *3D-IDEAS*)

B.2.2. Application à l'extraction des éléments parasites substrat

Dans les cas des hautes fréquences, les TSVs deviennent une source majeure de bruit de substrat, qui menace les performances des dispositifs voisins et qui augmente la consommation d'énergie. Donc, dans le cas de cette haute fréquence, afin de prévenir l'ensemble du système (filière, avec son « packaging ») contre les surtensions, les rebonds, ou oscillations parasites, il est important de comprendre les caractéristiques de ce couplage du substrat. La perte de la performance du circuit provoquée par le substrat en silicium peut être très forte. Compte tenu de la fréquence radio (RF), le substrat pourrait avoir, à certains nœuds d'intérêt, un comportement "RLC" (essentiellement un "RC" pour les basses fréquences).

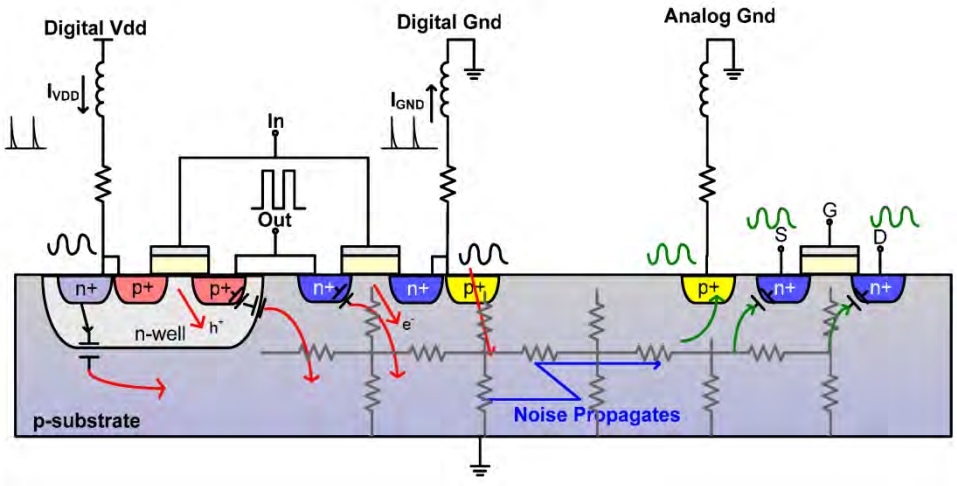


Figure B-13 Couplage du substrat dans les circuits à signaux mixtes [8]

De nombreuses techniques d'isolation pour le couplage substrat existent. Le bon choix parmi celles-ci est primordial pour le fonctionnement optimal du futur circuit mixte. En effet, les contraintes en début de conception d'un circuit sont nombreuses: boîtier, nombre de lignes d'alimentation disponibles, technologie microélectronique envisagée, surface de silicium maximale, structures d'isolation substrat possibles Le concepteur doit 'jongler' avec ces différentes contraintes afin d'optimiser au mieux le futur circuit. Les choix sont souvent effectués sans autre certitude que celle du concepteur.

Nous décomposons, dans une première approche, les sources de perturbations substrat en deux phénomènes distincts.

La première source de bruit substrat est globale, car elle est injectée sur l'ensemble de la surface d'un bloc numérique: il s'agit du bruit d'alimentation. La seconde source est locale, injectée de manière ponctuelle: il s'agit du couplage capacitif des signaux logiques, via les capacités MOS, drain/substrat ou métal/substrat, ou encore de l'ionisation par impact sous la grille des MOS. Ces deux phénomènes, un global et un local, peuvent être liés.

L'extracteur de parasites substrat, implémenté Matlab, mais aussi en langage Java pour une portabilité facilitée utilise les fonctions de Green afin de générer un maillage RC de ce substrat [167]. Le substrat est considéré comme une superposition de couches conductrices de différentes résistivités et de différentes permittivités diélectriques. A partir d'une liste de contacts, a priori de forme rectangulaire, l'outil « retourne » une matrice de résistances, ou de capacités. Le noyau utilisé prend en compte les bords de puce (cf. conditions aux limits); il est de la forme:

$$G(x,y,z,x',y',z') = \sum_{m,\,n\,=\,0}^{\infty} f_{mn} \,.\, \cos(\delta.x).\cos(\delta.x').\cos(\zeta.y).\cos(\zeta.y') \quad [167]$$

Cette fonction est une série en deux dimensions, indexées par m et n. F_{mn} est une fonction de m et n calculée à partir de la taille et du profil de conductivité du substrat; x et y sont les coordonnées du point où est appliqué un courant élémentaire; x' et y' les coordonnées du point où est induite par le courant élémentaire la tension substrat; δ et ς sont des fonctions de m et n calculées à partir de la taille du substrat considéré.

L'extraction du substrat se déroule en trois étapes, le logiciel se présente donc sous trois onglets différents. En premier lieu, il est nécessaire de décrire le substrat dans lequel se propagent les signaux parasites. Ensuite, il faut donner les différentes géométries du circuit: taille de la puce, localisation et forme des contacts substrat. Finalement, une fois les données utiles entrées dans l'outil, un dernier onglet permet de calculer les différentes valeurs de résistances et capacités parasites entre les contacts de surface du substrat. Figure B-14 résume l'utilisation de cet outil informatique:

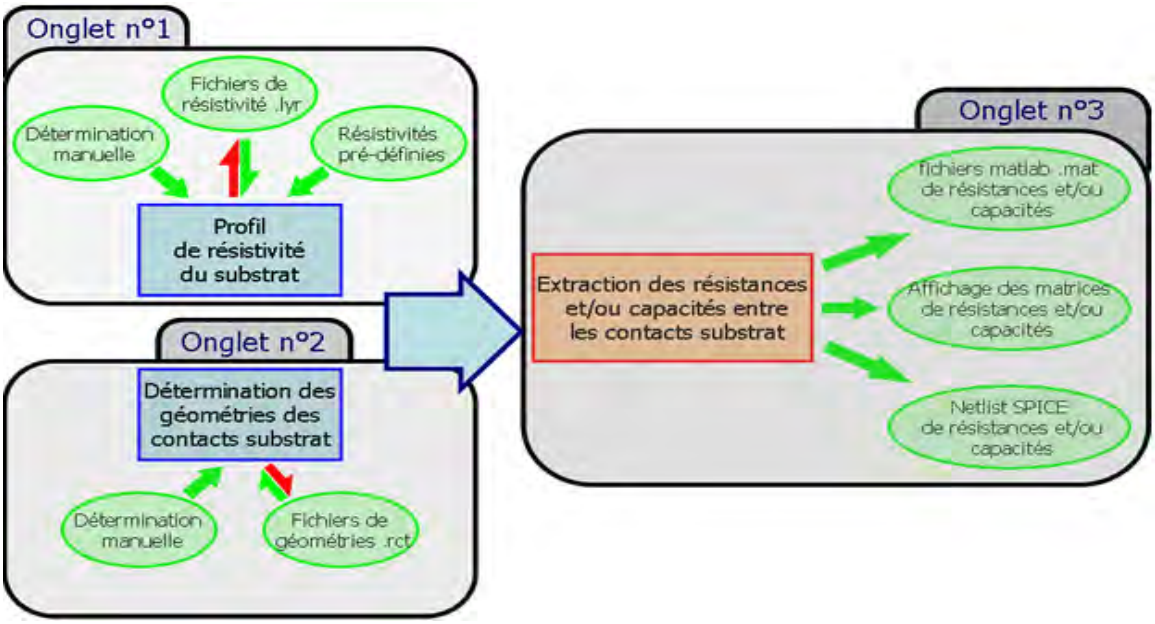


Figure B-14 Fonctionnement de l'outil informatique d'extraction des résistances et capacités substrat

Dans le cas de l'extraction du substrat par la méthode de Green, le substrat est considéré comme une superposition de couches diélectriques et/ou conductrices.

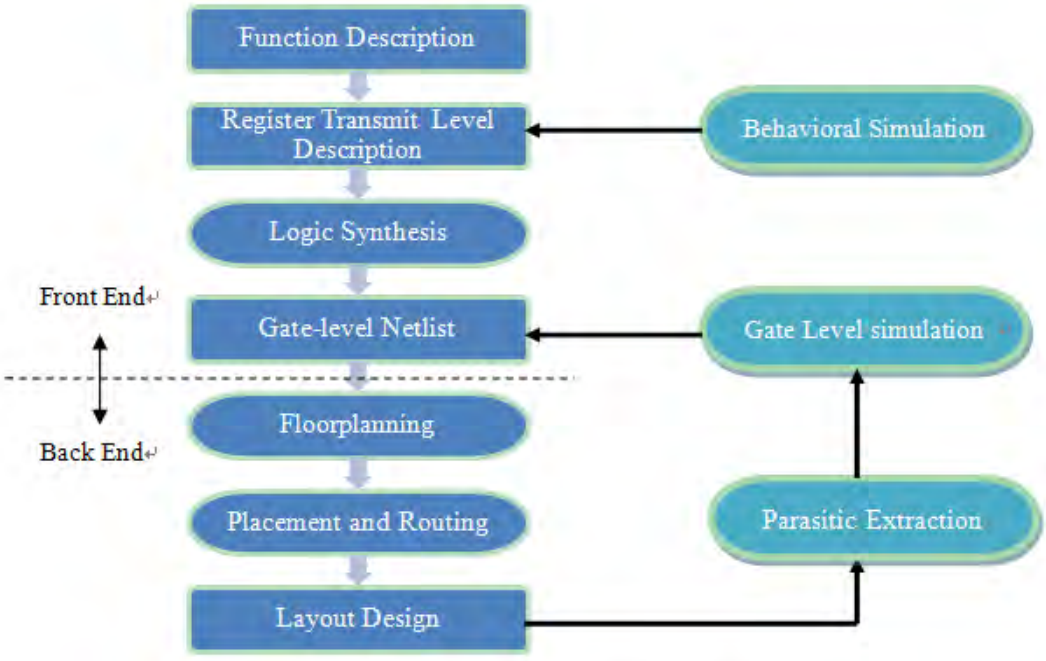


Figure B-15 Un processus technologique de conception typique d'IC

Un flux de conception de circuits intégrés est montré sur la Figure B-15. Comme on peut le voir dans le graphique, entre la conception de l'aménagement et de la simulation de circuit au niveau « composant », il ya une étape appelée «extraction de parasites». La tâche de cette étape est de construire un modèle de capacités, d'inductances, de résistances et d'autres composants pour l'étude de couplages électromagnétiques; une simulation précise de l'ensemble du circuit peut alors être réalisée. Capacité, résistance et inductance: parmi ces trois paramètres, la capacité est souvent la plus rédhibitoire, car elle affecte gravement les délais du circuit, la consommation d'énergie et de l'intégrité du signal. Dans le même temps, dans le circuit à haute fréquence, les effets d'inductance deviennent également très importants,

aussi bien les phénomènes de stress thermiques et mécaniques. Le courant de Foucault joue également un rôle important dans la fréquence radio (RF) de circuits. Une représentation intégrale pour les pertes par courants de Foucault sur un substrat conducteur est présentée dans [87].

Les travaux pionniers de la modélisation et de l'analyse du couplage de substrat dans les circuits intégrés (IC) ont été effectués par Ranjit Gharpurey [88]. Puis, par M. Ali Niknejad [90]: la fonction de Green doit être en outre transformée en une forme stable numériquement, appropriée a priori pour « résoudre » la matrice d'impédance pour un arrangement tridimensionnel arbitraire des conducteurs placés n'importe où dans le substrat. Puis, Zuochang Ye présentent un algorithme efficace pour l'extraction à trois dimensions (3-D) de capacité sur des substrats multicouches et avec perte [93]. Ce nouvel algorithme présente une amélioration par rapport à l'approche quasi-3-D utilisée dans les solveurs basés sur les fonctions de Green et prend en considération les flancs de conducteurs 3-D.

B.3 3D Impédance Extraction (3D-IE)

En raison d'une certaine inefficacité des méthodes numériques pour le modèle de substrat, des outils idoines sont nécessaires pour accélérer la conception de circuits, sans perte significative de précision et de fiabilité. L'outil doit être utilisé pour analyser la topographie, pour saisir le comportement électrique du circuit, et pour calculer la matrice d'impédance du substrat et son couplage avec la connectique. A ce sujet, certains programmes de recherche ont été publiés ces dernières années, orientés: électrique [37, 41], thermique [100], ou contrainte mécanique [101]-[54]. Une extraction du substrat (méthode BEM) a été proposée[38], mais elle est seulement appliquée pour analyser le couplage entre contacts établis sur la surface supérieure du substrat, pas pour des structures 3D-TSV. La capacité de couplage parasite est analysée dans différentes configurations dans [9], selon que le TSV soit entouré de fils d'interconnexion, les plus classiques ; en bas ou sur le côté. Cependant, le modèle TSV est simplifié en négligeant l'inductance TSV, la capacité de l'oxyde et en faisant l'hypothèse d'un substrat à haute résistivité. Ainsi, nous proposons une nouvelle méthode matricielle (TLM) [102, 103] basée sur le concept bien connu de la ligne de transmission; pour extraire l'impédance entre les contacts et/ou les TSVs, qui est applicable aux substrats multicouche.

Dans ce chapitre, cette nouvelle méthode, en s'appuyant sur la TLM sur substrat multicouches, est introduite. Elle peut modéliser les effets susdits dans le volume. Les détails de l'algorithme sont donnés pour calculer les paramètres Z entre des contacts « top » ou incorporés et des TSVs pour couches multi-support. Ensuite, cette approche de modélisation est validée dans la troisième partie en effectuant une analyse dans le domaine fréquentiel par les paramètres Z [104]. Enfin, la conclusion résume les points essentiels et les rapports sur des travaux en cours seront énoncés.

B.3.1. 3D-IE: Introduction

Comme décrit ci-dessus, l'intégration à haute densité d'un système à haute fréquence induit des couplages de bruit conséquents ; c'est l'une des considérations les plus importantes dans la conception, en raison de sa grande influence sur la performance des circuits intégrés. L'objectif principal de l'analyse de substrats 3D est d'extraire efficacement les paramètres d'impédance (Z) entre contacts et TSVs, qui se trouvent sur ou dans le substrat de silicium. Un outil d'extraction d'impédance efficace pour les contacts et TSVs pourrait aider le concepteur à accélérer la conception et optimiser la mise en page finale. Selon Ted Vucurevich, parmi

tous les défis EDA pour la conception SIC 3D, des outils et des méthodologies pour les tests IC 3D sont considérées comme le « défi n ° 1 »[105].

Comme dans les technologies planaires, les interconnexions 3D peuvent être appréhendées via des modèles électriques équivalents, type «RLCG» avec un réseau Π ou T. Souvent, un modèle compact simple a été construit pour la modélisation du substrat comme un nœud simple (Figure B-16(a)). Toutefois, cette hypothèse n'est viable que lorsque substrat est hautement conducteur, dans les domaines de basses et moyenn fréquences, et n'est pas adapté pour les substrats multicouches. Dans les hautes fréquences, les raccords du substrat peuvent devenir une source de bruit, ce qui peut conduire à des erreurs et des dysfonctionnements des systèmes, des retards dans l'ajustement du signal, une faible fiabilité et la courte durée de vie de l'équipement; par conséquent, les effets de substrat peuvent être prises en compte par la modélisation via un réseau «RLCG » (voir, par exemple la Figure B-16(b). C'est la raison pour laquelle une méthode d'extraction associée du substrat est nécessaire.

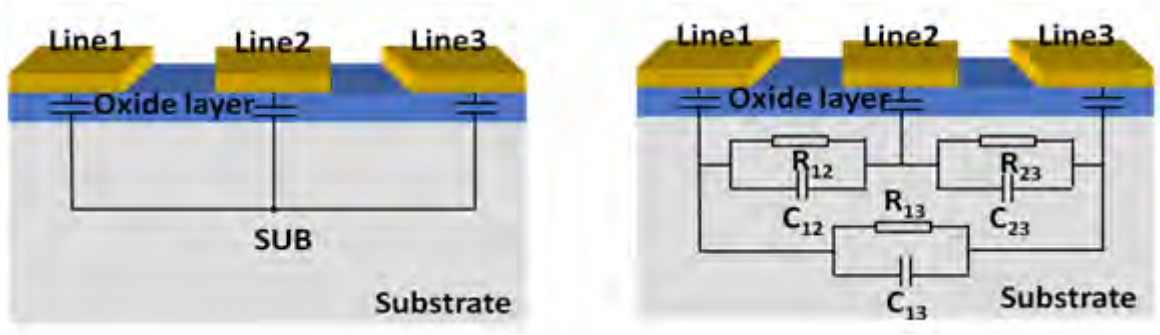


Figure B-16 (a) vue avant : TSVs moyenne densité et la modélisation, y compris le chemin des courants (b) la modélisation compacte 'RLCG' de la ligne de signal et une ligne de masse du guide d'ondes coplanaire.

B.3.2. Analyse d'Algorithme

En règle générale, les paramètres Z peuvent être définis comme

$$Z_{mn} = \frac{V_m}{I_n}\bigg|_{I_{k\neq n}=0} \tag{B.6}$$

En pratique, en injectant un courant d'excitation unitaire en un point n, on calcule la tension résultante au point m ; nous pouvons alors obtenir l'impédance Z_{mn} entre le contact m et le contact n directement.

Si nous pouvons obtenir la distribution potentielle résultant du substrat causée par le courant unitaire, nous pourrions obtenir les paramètres Z par l'équation (B.6) directement.

Dans des conditions quasi-statiques[168], le potentiel sur le substrat satisfait à l'équation de Laplace

$$\nabla^2\varphi(x,y,z) = 0 \tag{B.7}$$

Il peut aussi s'écrire

$$\left(\frac{\partial^2}{\partial x^2}+\frac{\partial^2}{\partial y^2}+\frac{\partial^2}{\partial z^2}\right)\varphi(x,y,z) = 0 \tag{B.8}$$

Après une transformée de Fourier rapide bidimensionnelle spatiale (FFT) [106] dans les directions x, y, nous transformons le domaine de coordonnées spatiales en un domaine fréquentiel [107], méthode largement utilisée, dans le traitement de l'image numérique.

Ainsi, l'équation ci-dessus est transformée en,

$$\frac{\partial^2 \Phi}{\partial z^2} - k_x{}^2 \Phi - k_y{}^2 \Phi = 0 \tag{B.9}$$

où Φ est le potentiel de domaine dans le fréquence spatiale et k_x, k_y sont les variables spatial-fréquences.

Après quelques transformations, nous obtenons :

$$\begin{cases} \dfrac{\partial \Phi}{\partial z} = -\dfrac{J_z}{(\sigma + j\omega\varepsilon)} \\ \dfrac{\partial J_z}{\partial z} = -(\sigma + j\omega\varepsilon)\left(k_x{}^2 + k_y{}^2\right)\Phi \end{cases} \tag{B.10}$$

Ces équations indiquent la relation entre la densité de courant dans la direction z et la répartition de potentiel dans le domaine spatial-fréquence.

Basé sur la méthode TLM, dans les réseaux à deux ports, dans le cas de l'onde harmonique, la tension u (z, t) et le courant i (z, t) peut être représentés comme suit.

$$\begin{cases} \dfrac{dU(z)}{dz} = -(R_0 + j\omega L_0)\cdot I(z) = -Z_1 I(z) \\ \dfrac{dI(z)}{dz} = -(G_0 + j\omega C_0)\cdot U(z) = -Y_1 U(z) \end{cases} \tag{B.11}$$

Comparant équation (B.10) et l'équation(B.11), nous constatons qu'ils sont formellement identiques les uns de autres.

La tension U de ligne dans la TLM correspond à la distribution de potentiel transformée Φ et les courants de ligne I correspond à la composante z de la densité de courant dans le domaine transformé J_z. Cela veut dire que le problème de l'analyse du substrat peut être lié à un problème de ligne de transmission équivalent.

Pour un modèle de substrat à une seule couche, la relation entre le modèle de substrat et sa ligne de transmission équivalente est représenté sur la Figure B-17 (remarquez le sens du courant de I_2', sortant du port: noté I_2' pour le distinguer du courant injecté I_2).

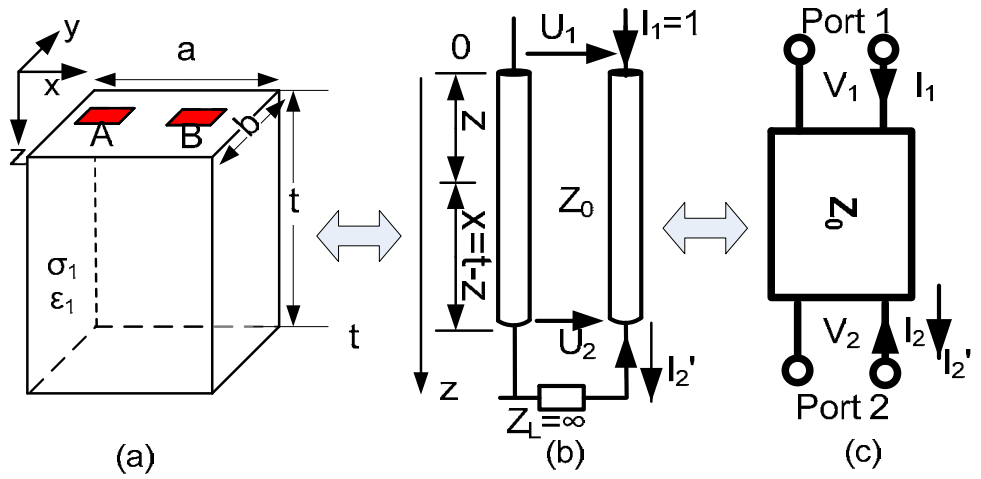


Figure B-17 (a) présente deux contacts prévus sur la surface supérieure d'un substrat à couche unique. (b) Son modèle de ligne de transmission de TLM équivalent. (c) Équivalent modèle de réseau à deux ports. Étant donné que le courant qui circulent sur la surface inférieure (a) est égal à zéro, de sorte que l'impédance de charge (ZL) à (b) est l'infini positif.

Un substrat en couche unique pourrait être modélisé comme un réseau à deux ports, un système multicouches comme en Figure B-18 (a) peut être modélisée comme la connexion en cascade des réseaux à deux ports (Figure B-18 (b)).

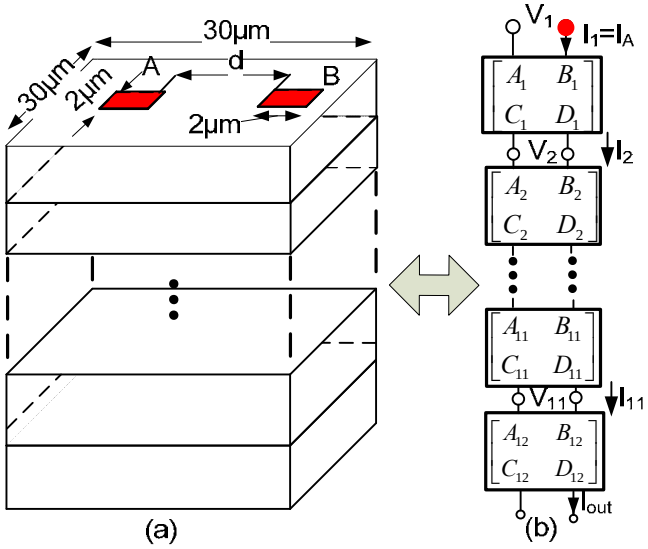


Figure B-18 Multicouches avec contacts de surface à tester (a) et son modèle TLM correspondant (b). La dimension du substrat est de 30 microns, 30 microns dans les directions X, Y. Deux contacts carrés de 2 microns × 2 microns sont situés sur la surface supérieure de ce substrat à plusieurs couches avec une distance de séparation d.

Les paramètres Z peuvent être convertis à partir des paramètres ABCD (cf. matrice chaîne) de l'équation(3.36).

$$Z = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} = \begin{bmatrix} \frac{A}{C} & \frac{\det(ABCD)}{C} \\ \frac{1}{C} & \frac{D}{C} \end{bmatrix} \tag{B.12}$$

Puis Z_{11} utilisé comme Z_{in} peut être obtenu à partir de l'équation(B.12). Ensuite, nous pouvons connaître le paramètre Z.

La principale force de la « 3D-IE », c'est qu'elle est bien dédiée aux contacts intégrés. Deux cas différents, contacts partiels intégrés et tous les contacts enfouis, seront discutés.

Le schéma pour un contact intégré dans un substrat à trois couches est présenté sur la Figure B-19.

Comparaison avec la Figure B-18: la condition limite est la même, à savoir I_{out} = 0 et I_1 = 1. En raison que le contact B n'est pas situé sur la surface supérieure, ce que nous devons savoir, ce n'est pas la tension V_1 comme le modèle de la Figure B-18 mais la tension V_3 correspondant à la Figure B-19.

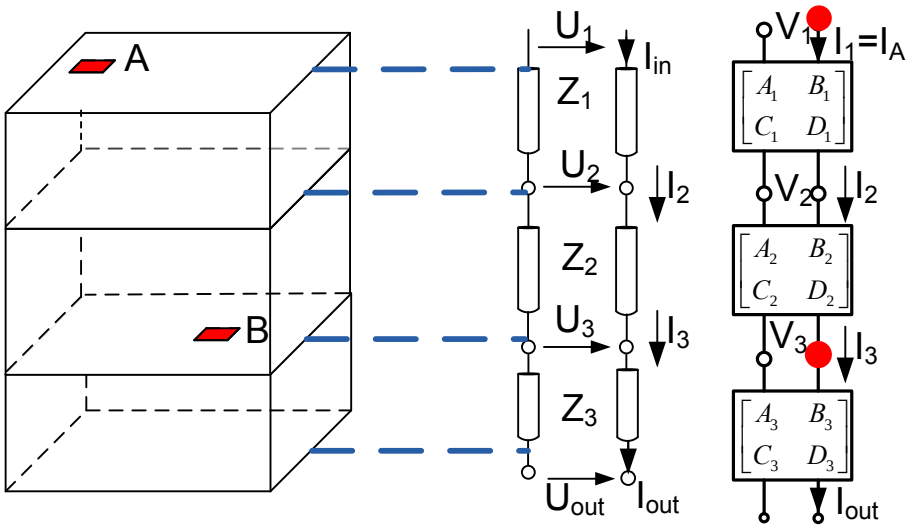


Figure B-19 Modèle pour certains contacts intégrés

Tandis que nous obtenons les paramètres ABCD pour chaque couche, V_3 peut être obtenu facilement sous la condition de I_{out}=0 et I_1=1. Puis Z_{31} est calculé « en » V_3 et I_1.

Utilisation de Z_{31} pour calculer le potentiel dans le domaine spatial-fréquence: une transformée de Fourier spatiale bidimensionnelle inverse est appliquée pour obtenir la distribution de potentiel réelle (φ_z) du plan xy sur lequel le contact B est posé. Ensuite, l'équation (3.1) est appliquée pour calculer Z_{BA}. Les autres éléments de paramètres Z peuvent être obtenus de manière similaire.

Si tous les contacts sont enfouis, le substrat peut être considéré comme une mise en parallèle de deux parties distinctes, comme indiqué dans Figure B-20.

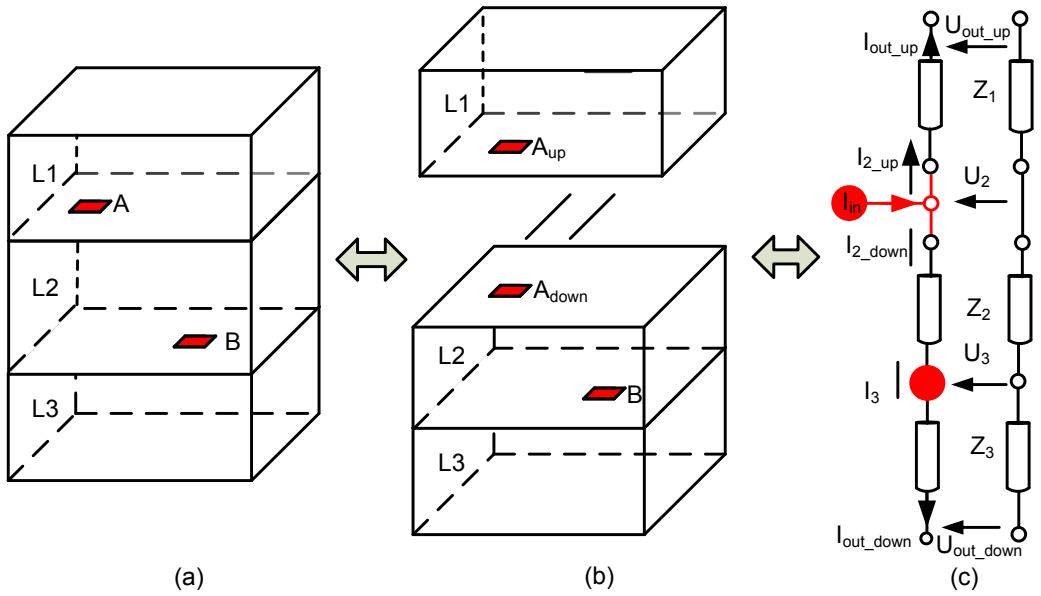


Figure B-20 Modèle pour tous les contacts intégrés

Le courant est injecté au niveau du contact A, de sorte que le substrat est divisé en deux parties, à partir de la couche (Figure B-20(b)). Le modèle TLM équivalent est comme indiqué à la Figure B-20 (c). Le I_{out_up} et I_{out_down} sont tous égaux à zéro en raison de la condition aux limites [104]. I_{in} est un courant unité (I_{in} = 1). Afin d'obtenir l_{Z32}, ce que l'on doit connaître c'est la tension V_3. Pour le modèle TLM substrat de la moitié supérieure, supposons que l'impédance d'entrée est Z_{in_up} et au niveau de la moitié inférieure : Z_{in_down}, en raison de la mise en parallèle (cf. diviseur de courant),

$$I_{2\_down} = I_{in} \frac{Z_{in\_up}}{Z_{in\_up} + Z_{in\_down}} \tag{B.13}$$

Les impédances Z_{in_up} et Z_{in_down} peuvent être calculées via les paramètres ABCD de chaque couche comme le montre la Figure B-20(c). Comme on calcule I_{2_down}, le modèle sera le même modèle que dans la Figure B-19. Les étapes suivantes sont exactement les mêmes avec les contacts partiels du modèle intégré.

En utilisant cette méthode, le potentiel de chaque couche peut être calculé. La Figure B-21 montre le potentiel d'un substrat avec deux contacts dans une couche 6 et l'autre dans la couche 9.

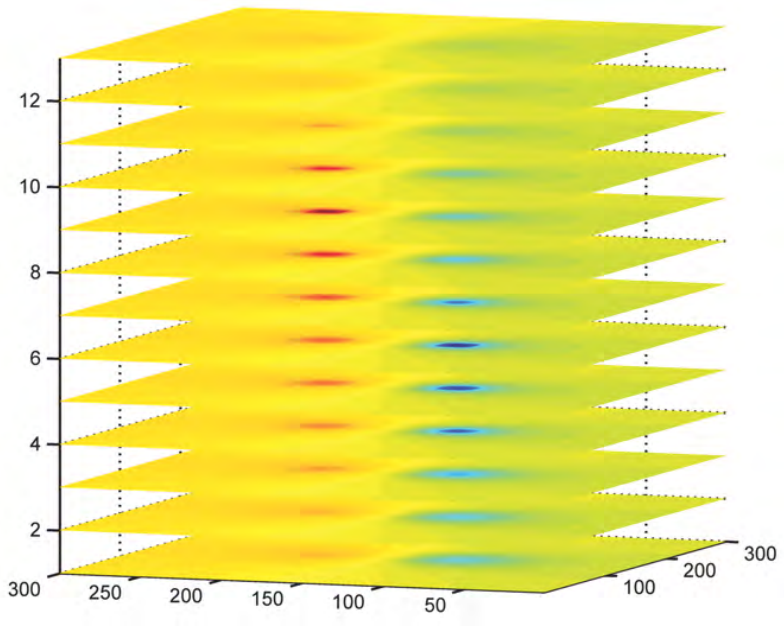


Figure B-21 Potentiel de chaque couche

Grâce à notre analyse ci-dessus, on peut calculer l'impédance entre des contacts portant sur des emplacements arbitraires et des couches arbitraires. Ainsi, afin de calculer l'impédance impliquant des TSVs, on considère une structure spéciale, comme indiqué en Figure B-22 (a).

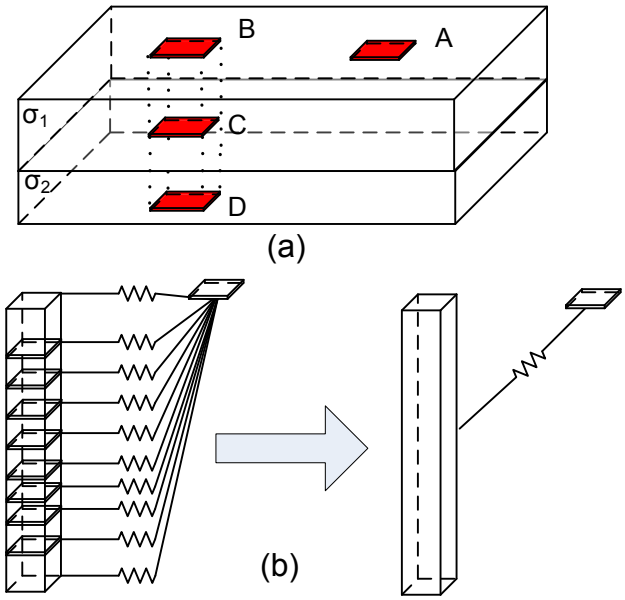


Figure B-22 Modèle équivalent TSV et contact

Les impédances entre AB AC et AD peuvent être calculées par l'algorithme ci-dessus. Ensuite, nous combinons le couplage entre AB AC et AD pour obtenir un couplage entre le contact A et le contact "BCD". En fait, le «contact BCD", la combinaison de B, C et D, est le TSV (ici, nous supposons que le TSV n'est pas entouré par un revêtement d'oxyde, le cas du TSV avec revêtement d'oxyde sera discuté plus tard). Un schéma est représenté en Figure B-22(b).

On peut diviser le TSV en petites trongonnage parties, et examiner ensuite chaque partie comme un contact et utiliser le processus ci-dessus pour obtenir l'impédance entre chaque

petite partie TSV et les contacts. Enfin, combiner toutes les impédances pour obtenir l'impédance finale entre le TSV et le contact, comme indiqué dans Figure B-22(b).

Grâce à un algorithme similaire, l'impédance entre TSV et TSV peut être calculée en divisant à la fois les TSVs en petits morceaux. Après avoir obtenu l'impédance entre chacun des «morceaux» des deux TSVs, l'impédance totale entre 2 TSV peut être obtenue en combinant tout l'impédance.

Ainsi, le processus général de l'algorithme est exprimé comme sur la figure ci-dessous.

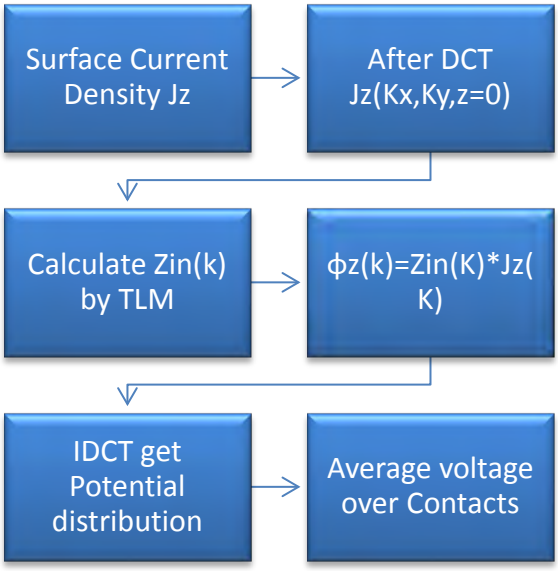


Figure B-23 Les étapes générales de l'algorithme (IDCT : Inverse DCT)

B.3.3. Validation du Modèle

L'impédance paramètre Z, d'un substrat multicouche, sera extraite par 3D-IE et la méthode des éléments finis (FEM), respectivement.

Tout d'abord, l'impédance sera calculée exactement par notre algorithme ci-dessus. Pour la simulation numérique, nous utilisons COMSOL, un simulateur multiphysique bien connu et robuste (électrique, thermique, contraintes mécaniques ; couplages) [104], c'est aussi un outil dédié pour l'analyse électromagnétique. Il utilise essentiellement des algorithmes de type Galerkin [111]. Typiquement, une simulation 3D peut utiliser quelques dizaines de minutes, voire quelques heures.

Dans notre méthode nous injectons une densité de courant constant à tout point de calcul au niveau du contact, nous utilisons le théorème de Millman [112] qui est appliqué partout dans le contact. La tension de contact est la valeur moyenne des tensions des éléments de contact discrets, calculée par:

$$V = \frac{\sum_{n=1}^{N} j\omega c\varphi_n}{\sum_{n=1}^{N} j\omega c} = \frac{1}{N}\sum_{n=1}^{N}\varphi_n \qquad \text{(B.14)}$$

où φ_n est la tension de substrat au niveau d'un nœud, et N est le nombre de points du contact. Ainsi, la plaque de substrat est considérée comme une injection de la densité de courant constante et non un potentiel uniforme.

Nous sommes très conscients que le cadre de la modélisation quasi-électrostatique ne peut pas fonctionner si parfaitement jusqu'à 10THz (contre des expériences), ce qui implique une longueur d'onde d'environ dix um pour le Si; cette longueur d'onde est du même ordre de grandeur des distances inter-contacts. Actuellement, nous n'avons pas pris en compte explicitement la perméabilité, il n'est pas réaliste d'aller au-delà de 200GHz (nos manipulations n'excèdent pas 20 GHz) dans cette analyse , mais nous pensons qu'il est intéressant de comparer, ab inition, la méthode des éléments finis pour tester la robustesse de notre algorithme (but initial).

Comme exemple, une région P+ /P d'un process BiCMOS 0.35µm est choisie, et décomposée en douze couches de bas en haut avec une épaisseur de t1, t2 ... t12 et une conductivité de σ1, σ2 ... σ12 qui sont indiquées sur la Figure B-24 et Figure B-25. La permittivité relative de toutes les couches est de 11,9.

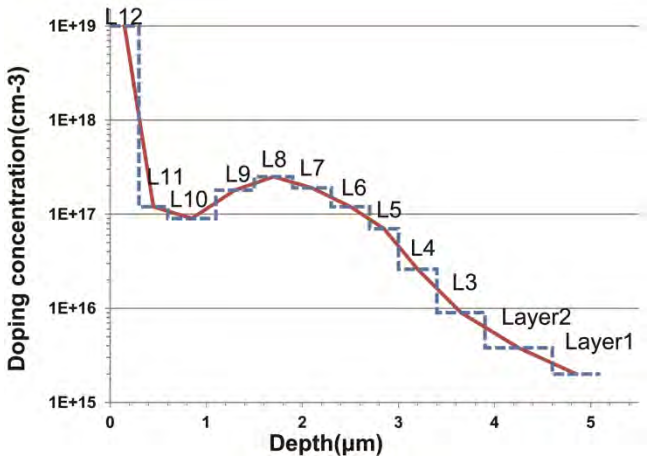


Figure B-24 Profil de dopage : technologie 0.35µm (p^+/p- region)

La caractéristique en fréquence de l'impédance sera recherchée dans le domaine fréquence de 10^8Hz à 10^{13}Hz et la distance dans la direction X entre les contacts (ou TSVs) varie de 1µm à 16µm.

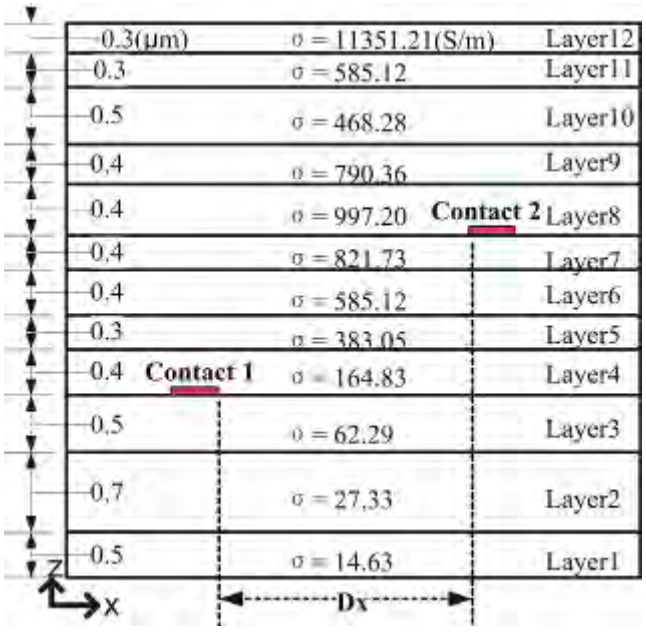


Figure B-25 Caractéristique de la géométrie du substrat dans la direction Z (épaisseur) et la propriété physique (conductivité) avec deux contacts intégrés, ; la permittivité relative est toujours de 11,9. Contacts enfouis en couche 4 et couche 8. Les dimensions dans la direction X et Y pour le substrat et les contacts sont les mêmes que sur la Figure B-18 (a)

Un contact est noyé dans la surface inférieure de la couche 4 et l'autre est présent sur la surface inférieure de la couche 8. Comme le test ci-dessus pour les contacts de surface, la distance de séparation latérale (Dx) des contacts est de 6 microns et la fréquence de $1e^{8}$ à $1e^{13}$Hz. En vue de l'analyse, deux paramètres du port COMSOL différents sont appliqués : la densité de courant constante (CD Constante) qui injectent une densité de courant uniforme à l'orifice de contact et de tension constante (constante V) qui injectent une tension uniforme au contact. Les résultats en fréquence de ces trois méthodes sont montrés sur la Figure B-26(a). D'après les résultats de la Figure B-26(a), on trouve un bon ajustement des caractéristiques en fréquence pour la méthode « COMSOL CD Constant ».

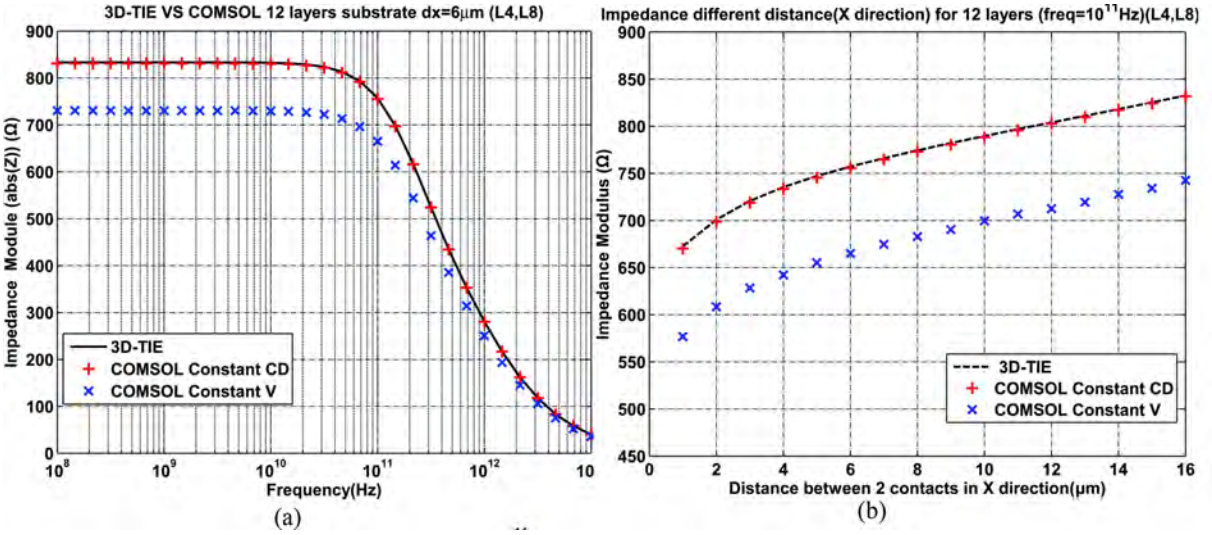


Figure B-26 (a) Impédance de 12 couches substrat avec la distance de séparation Dx = 6 microns pour les deux contacts qui sont noyés dans le substrat. Un est dans la couche 4 et l'autre dans la couche 8. Les résultats sont le module de l'impédance : a) Dx=6 μ; (b) module de l'impédance pour différentes distances entre des contacts. (f = 10^{11} Hz)

Figure B-26 (b) représente les résultats d'impédance avec la distance de séparation des contacts variable, à la fréquence de 1e11Hz.

La distribution de potentiel de la surface supérieure du substrat est présentée sur la Figure B-27. Les résultats de 3D-IE et COMSOL concordent très bien les uns avec les autres.

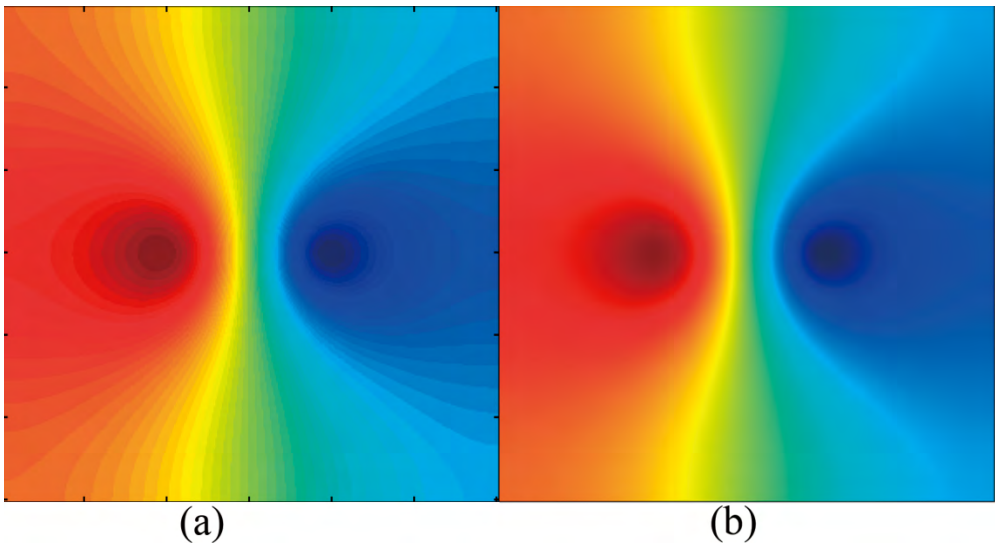


Figure B-27 Potentiels de surface du substrat obtenus à partir de 3D-IE (a) par rapport à COMSOL (b), pour les contacts incorporés dans le substrat à 12 couches, dans la couche 4 et la couche 8.

Basé sur le modèle des contacts, on extrude l'un des contacts dans le substrat pour obtenir un TSV de 5.1µm qui s'étend de la couche 12 à la couche 1 ; le modèle de contact TSV est montré Figure B-28(a).

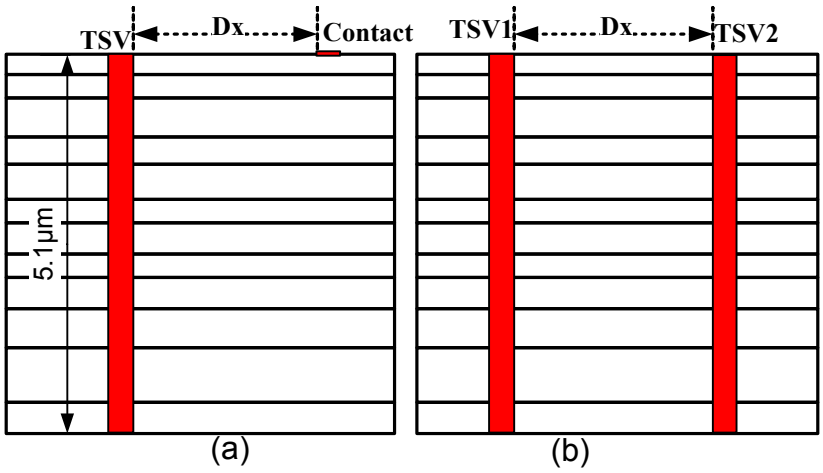


Figure B-28 Schématique du modèle (a) TSV-Contact et (b) TSV TSV-modèle. La dimension de la TSV est 2µm × 2µm × 5.1µm en X, Y et Z

De la même manière, la distance de séparation des TSVs est fixée à 6 microns et la fréquence varie de $1E^8$ à $1e^{13}$Hz. Les résultats de la Figure B-29(a) et de la Figure B-29(b) montrent un bon ajustement des caractéristiques en fréquence pour la méthode proposée et COMSOL quant à la résistance et la réactance respectivement. La méthode "New Material" de COMSOL peut considérer en fait une conductivité anisotropique ; ce nouveau matériau du via a la même conductivité que celle du cuivre dans la direction Z, mais a la conductivité de celle des couches de substrat Si dans la direction X et Y (dans notre méthode analytique, nous avons bien , actuellement, des conductivités latérales au niveau du via: ε_{SI} (en fait dans ces directions x,y , il existe l'effet capacitif de l'oxyde, mais aussi d'une possible zone désertée de silicium jouxtant la couche d'oxyde, et cela d'autant plus que le dopage est faible) . La méthode classique de COMSOL prend, quant à elle, pour le via, une conductivité isotropique, ici celle du cuivre (par défaut $\varepsilon_{Cu}=\varepsilon_0$) . Nous devrons prendre en compte plus finement ces aspects.

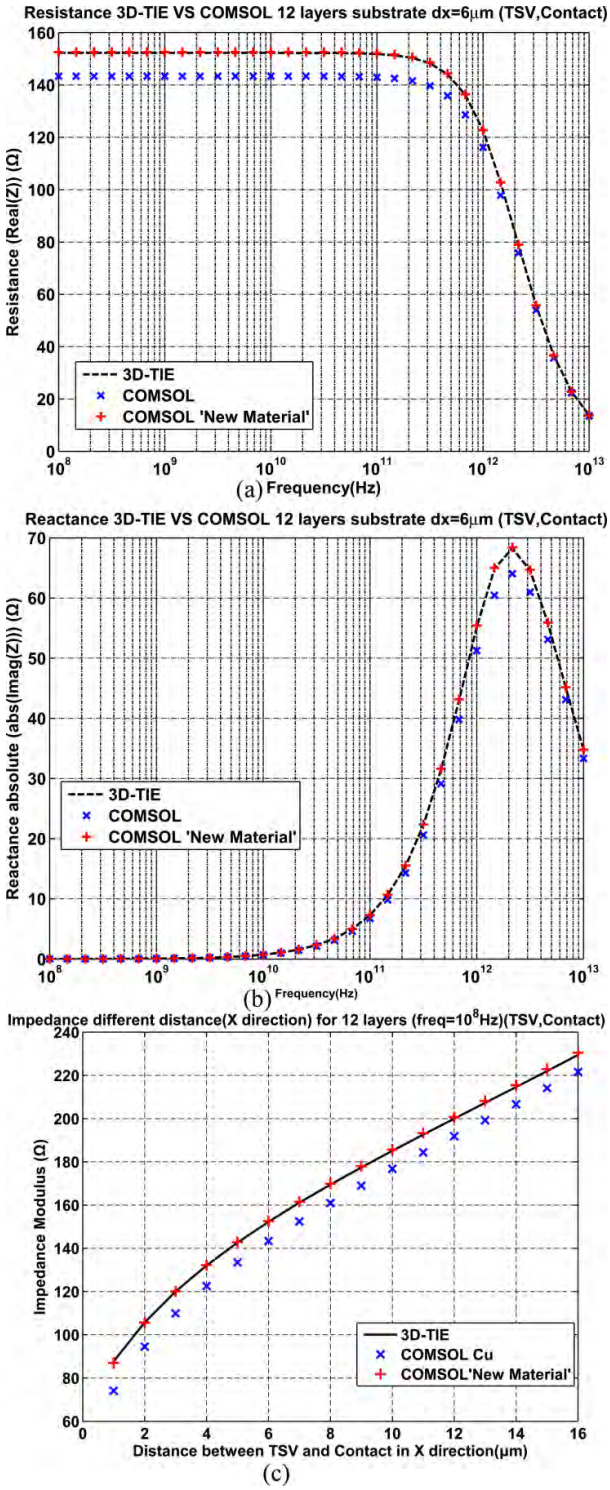


Figure B-29 Résistance (a) et valeur absolue de la réactance (b) de la 3D-IE et COMSOL entre TSV et le contact dx = 6 microns sous les fréquences allant de de $1e^8$Hz à $1e^{13}$Hz.

Deuxièmement : modifier la distance « contacts » Dx - Figure B-28 (a)- de 1 μm à 16 μm, pour une fréquence égale à $1e^8$Hz et tester l'impédance entre TSV et contact. Le matériau à conductivité anisotrope est également utilisé pour comparaison. Figure B-29 (c) montre un bon accord entre notre méthode et la simulation COMSOL « New material ». Figure B-30 présente le potentiel entre TSV et contact, de COMSOL utilisant le matériau anisotrope.

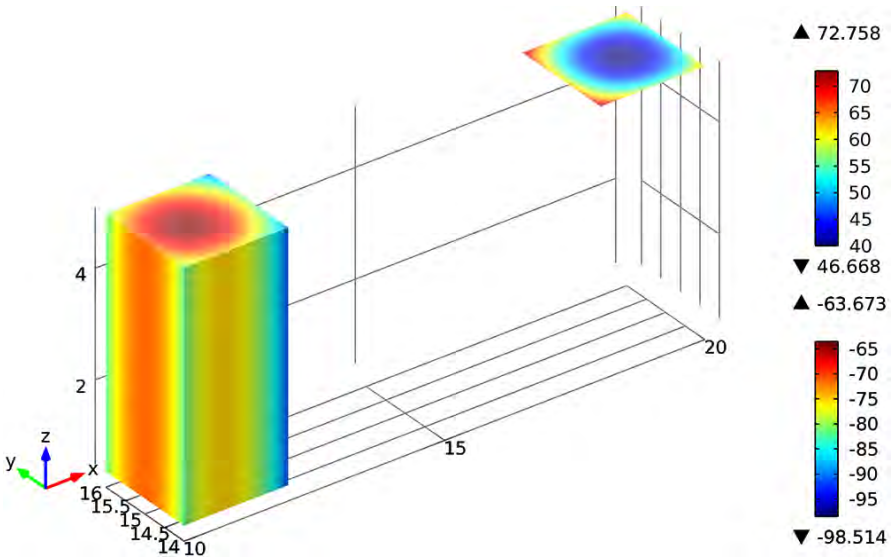


Figure B-30 Potentiel: modèle TSV-contact avec un TSV dans une matière anisotrope, qui a la même conductivité que le cuivre dans la direction Z et a les mêmes composantes de conductivité que le substrat de silicium dans les directions X et Y.

Basé sur le modèle contact TSV : extrusion verticale de deux contacts pour obtenir deux TSVs-, qui s'étendent de la couche 13 à la couche 1 : un modèle TSV-TSV peut être construit ; sa coupe étirée est illustrée à la Figure B-28 (b).

On fixe la distance de séparation à 6 microns, la gamme de fréquence s'étendant de 10^8Hz à 10^{13}Hz (voir la Figure B-31(a). Et l'on fixe la fréquence à 10^8Hz, modifiant la distance entre les deux TSVs de 1µm à 16µm ; on extrait l'impédance entre les deux TSVs. Les impédances (COMSOL et 3D-IE) résultant de cette extraction TSV, pour ces distances variables, sont présentées en Figure B-31(b).

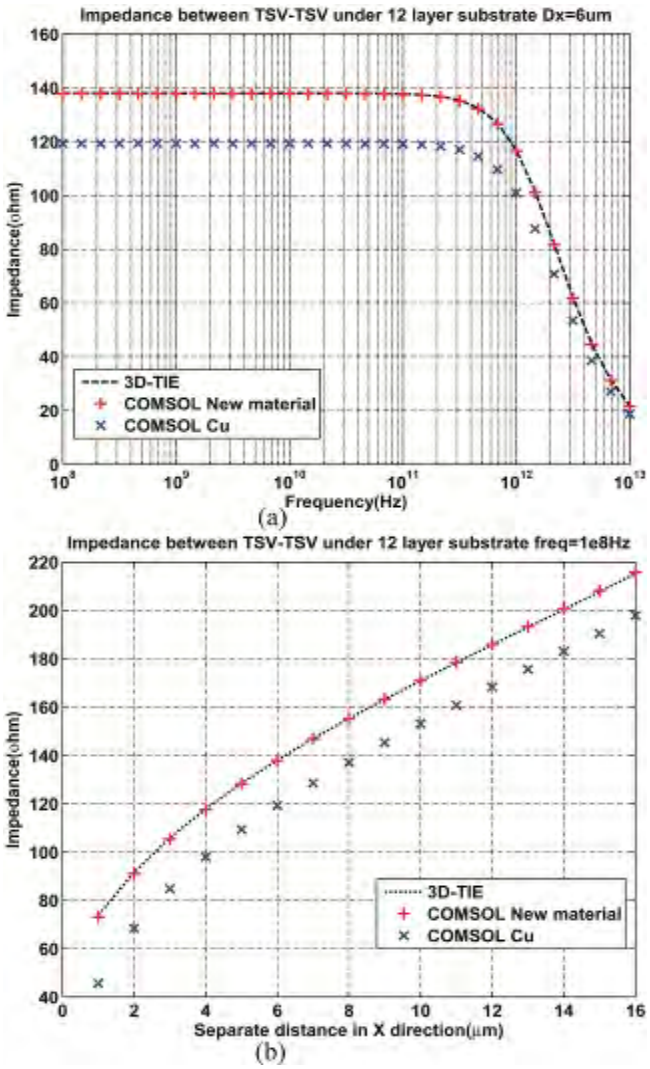


Figure B-31 Module de l'impédance : 3D-IE et COMSOL entre TSV ; a) en fonction de la fréquence avec Dx = 6 microns, (b) Impédance pour différentes séparations de TSVs 3D-IE vs COMSOL

En pratique, le TSV a une couche d'oxyde, d'isolement, de sorte qu'uun modèle amélioré est proposé : voir la Figure B-32.

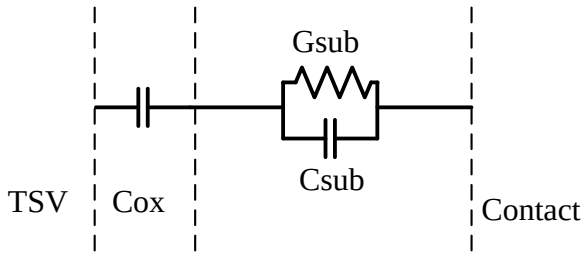


Figure B-32 Amélioration du modèle équivalent de couplage entre TSV et le contact

A comparer avec l'ancien schéma, un effet de capacité est ajouté à chacun des morceaux du TSV comme le montre la Figure B-33 (à terme, nous rajouterons, le cas échéant, pour les faibles dopages, une capacité de désertion, dans le silicium, en série avec cette capacité d'oxyde).

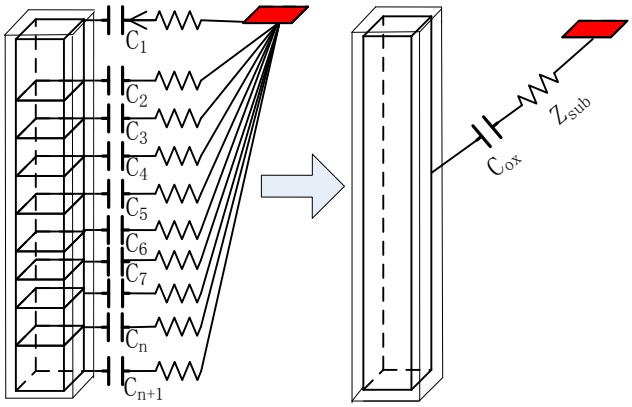


Figure B-33 Schéma de modèle de TSV/contact, dans lequel le TSV a un revêtement d'oxyde. Cox est la capacité de la couche d'oxyde entourant la TSV; Zsub est l'impédance du substrat.

Donc, l'étape investigation est, d'une part, le calcul de la capacité provoquée par la couche d'oxyde, d'autre part, l'insérer correctement dans le modèle.

A la différence de l'autre méthode basée sur les noyaux de Green(cf. [122]), qui ne peut calculer que pour des contacts rectangulaires, 3D-IE peut être utilisé de façon plus « souple » ; par exemple, utilisant disque, couronne, un rectangle, en boucle, en forme de T et ainsi de suite. La figure suivante montre quelques exemples soumis à notre 3D-IE.

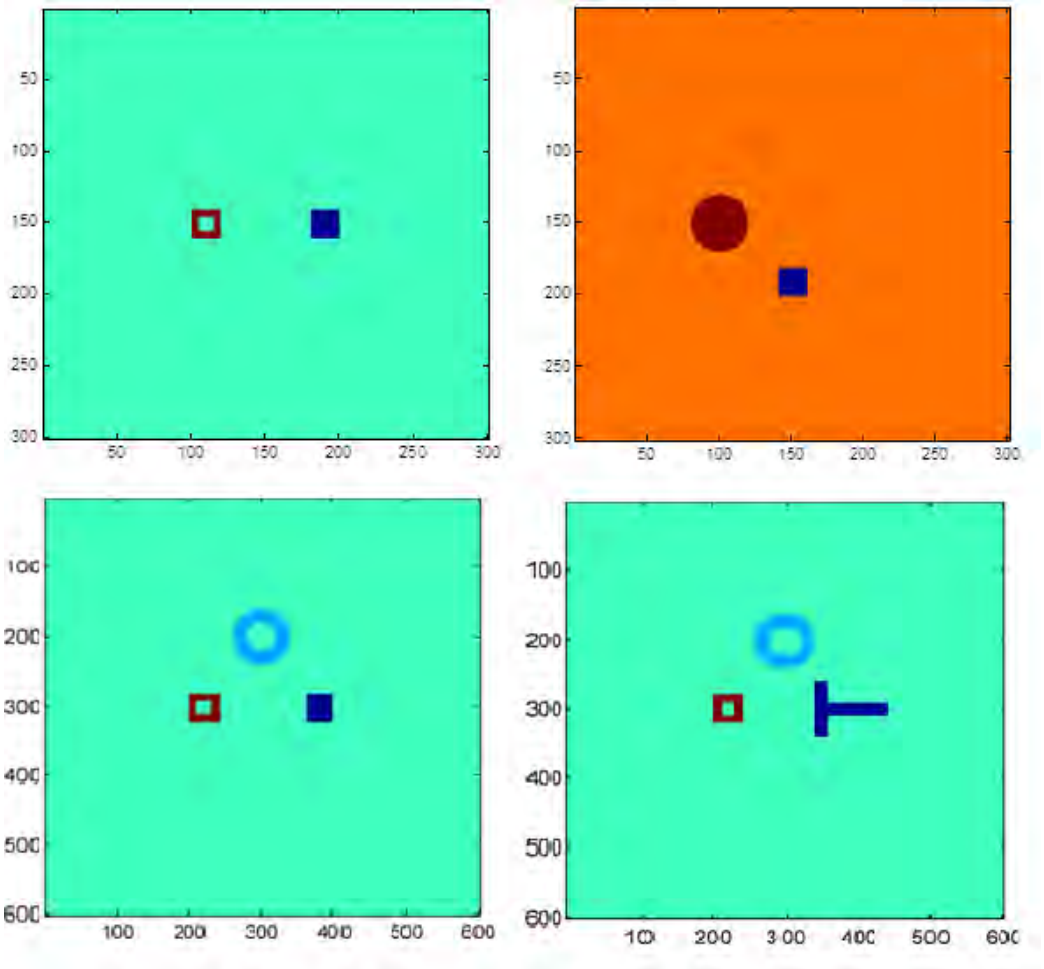


Figure B-34 Différentes formes de contacts qui peuvent être considérées en 3D-IE.

S'il y a des tranchées et / ou des puits dans un substrat, l'hypothèse d'homogénéité de la couche devient invalide, et la fonction de Green ne peut pas être utilisée directement. L'extraction du couplage du substrat traditionnel basé sur la technique de fonction de Green est limitée aux structures planaires et il est généralement difficile de développer des modèles analytiques pour gérer des variations latérales de la constante diélectrique.

Une approche (basée sur le théorème de superposition - Figure B-35 -) est proposée par Ranjit Gharpurey [60] et étendue à trois dimensions par Chenggang Xu [123].

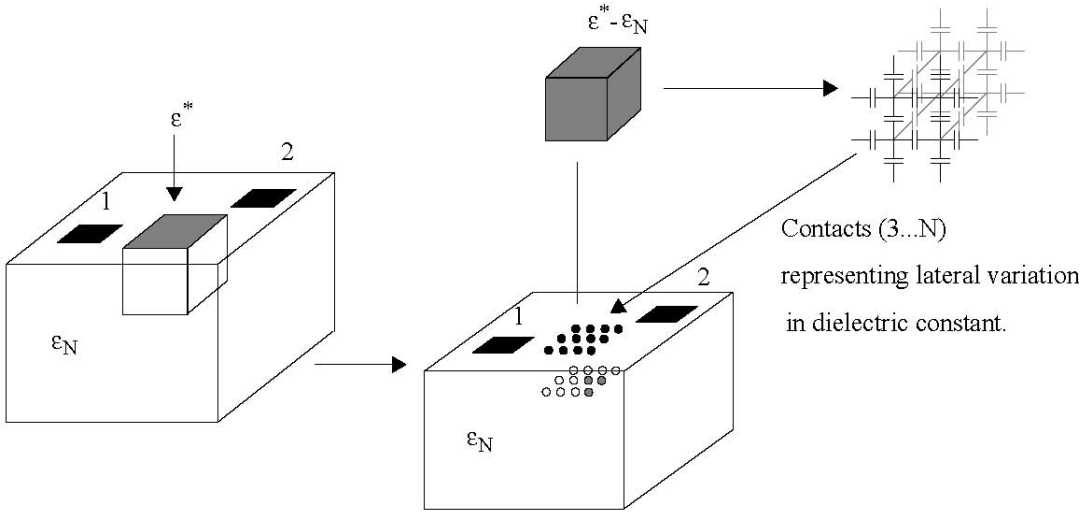


Figure B-35 Une technique pour modéliser une variation latérale des constantes diélectriques [122]

B.4 Interconnexions: modèles compacts

B.4.1. Introduction

Comme indiqué dans les chapitres un et deux, les technologies planaires 2D rencontrent de nombreux défis; en conséquence, l'intégration 3D est considérée comme une solution plus prometteuse. Toutefois, en raison de l'intégration dense élevée, l'intégration 3D implique que le contexte électrique d'ensemble doit être considéré comme des chemins de courant ou des couplages entre les éléments de puces. Ainsi, afin d'évaluer avec précision les performances du système 3D dans le processus de conception, les modèles compacts électriques sont notamment nécessaires pour la 3D interconnexions.

Dans ce chapitre, les modèles compacts d'interconnexion 3D sont proposés, notamment à densité moyenne de TSV, fiable pour les fréquences basses et « moyennes » (jusqu'à 20 GHz). Les simulations électromagnétiques 3D paramétriques et les extractions sont réalisées sur des structures de test. L'approche de modélisation que nous proposons est également présentée dans notre document soumis [126]. Ce procédé d'extraction est validé expérimentalement dans le cas d'un guide d'ondes coplanaire déposé sur un substrat à haute résistance. Les comportements RF des structures d'essai sont également étudiés. Enfin, la conclusion résume les points essentiels du chapitre et décrit les travaux futurs.

La modélisation électrique, dans un contexte mondial, sera illustrée dans cette partie pour les cas des guides d'ondes coplanaires et des chaînes TSV. Alors que le substrat est hautement conducteur pour les guides d'ondes coplanaires qui nous ont été soumis (cf ; CEA-LETI), il peut être modélisé comme une résistance très faible, voire un nœud simple. Pour chaque ligne coplanaire, le trajet de courant vertical dans la couche épitaxiale est modélisé par une résistance (Repi) en parallèle avec une capacité (Cepi). La modélisation de

l'environnement contient également les capacités de la couche d'oxyde (Cox) isolant les lignes du substrat.

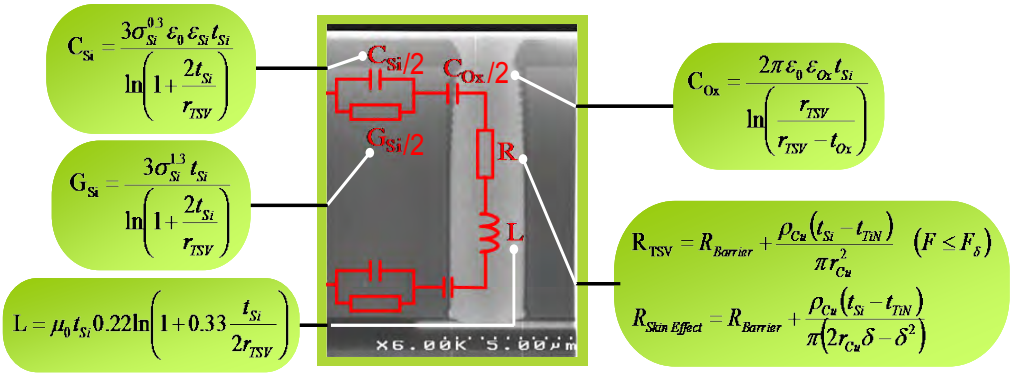


Figure B-36 Un modèle analytique à haute densité TSV ([129])

Parce que les descriptions des systèmes peuvent devenir complexes lorsque l'on considère le contexte électrique et la distribution de modèles compacts, nous avons donc développé sous Matlab ® [133] un outil 3D d'extraction, 3D TLE (transmission 3D Ligne Extractor), basé sur notre approche de modélisation et qui intègre l'algorithme d'extraction substrat (Figure B-37). Grâce à une syntaxe hiérarchique et des déclarations spécifiques, l'utilisateur décrit dans un fichier texte les données géométriques et technologiques, en définissant : ses couches, le type des éléments compris dans le système, la connectivité entre les éléments qui sont des composants « instanciés », et des interactions d'élément (couplage, interactions avec les couches pour la modélisation de la circulation des courants).

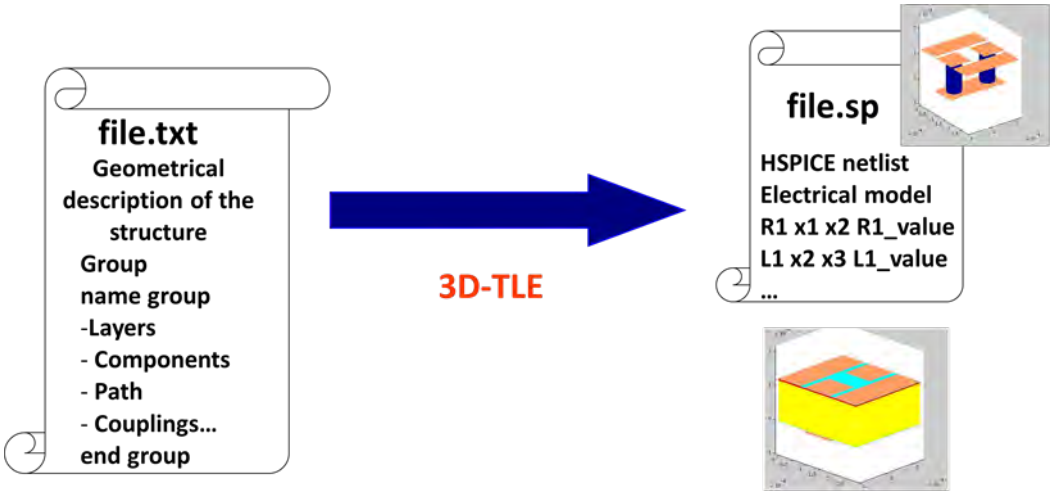


Figure B-37 Environnement de l'outil 3D TLE (3D Transmission Ligne Extractor)

L'outil d'extraction génère à partir de ce fichier texte une « netlist » de type SPICE, contenant le système RLCG, la description électrique, exportable vers les outils de CAD tels que Agilent Technologies ADS® [134]. La viabilité de notre 3D TLE a été vérifiée par des comparaisons de paramètres S pour les systèmes de données entre leurs netlists SPICE 3D TLE et leurs schémas conçus sous ADS®. Comme attendu, les résultats montrent que les réponses sont « les mêmes », mais décrire la structure en utilisant 3D TLE est plus facile et plus rapide que la conception à l'aide d' outil de CAD. 3D TLE fournit également l'image 3D du système.

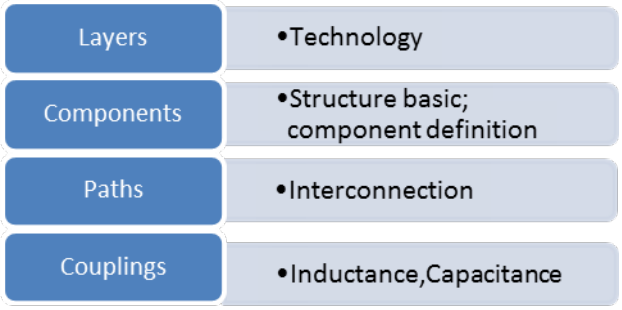


Figure B-38 Structure d'un fichier texte permettant de définir un structure substrat spécifique.

B.4.2. Validation: Structures de test

À première, une structure simple pour guide d'ondes coplanaires (CPW) est testée comme indiqué dans la suite de la Figure B-39.

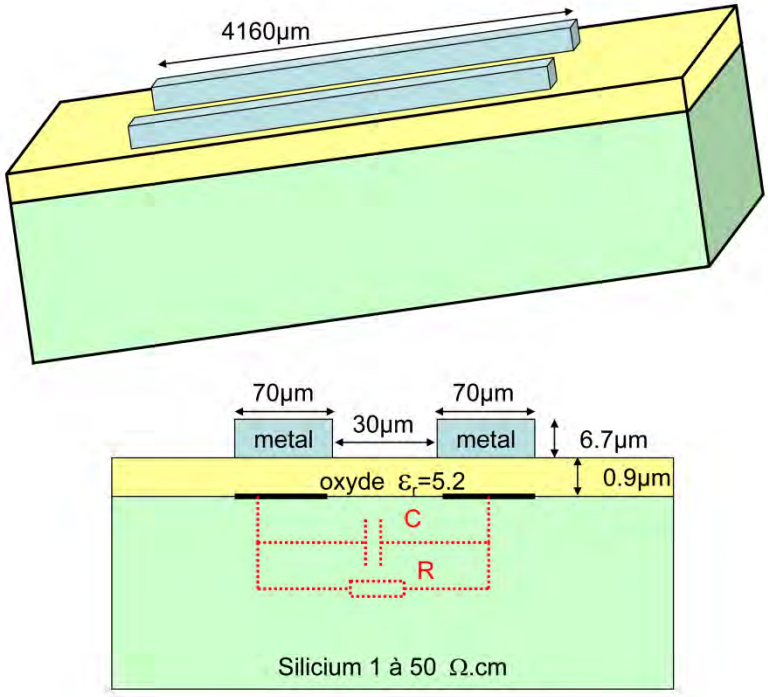


Figure B-39 Schéma d'une structure CPW utilisé pour tester (Source: LETI)

La modélisation est validée dans le domaine de fréquences RF via des comparaisons de paramètres S entre les mesures effectuées sur les structures de test, pour deux configurations différentes et les résultats de simulation de leurs modèles électriques équivalents. Les structures de test utilisées seront présentées dans un premier temps, puis la comparaison entre le test et la simulation sera donnée.

La structure est une structure en U telle qu'on a une ligne signal au niveau RLD connectée à 2 TSVs remontant jusqu'au niveau BEOL où se situent deux lignes de masse. Les lignes de masse, en cuivre, sont localisées de part et d'autre du point d'accès BEOL des TSV. Le substrat est recouvert d'une couche épitaxiée à laquelle s'ajoute une couche d'oxyde de silicium permettant d'isoler les lignes de cuivre du substrat. De même, une couche de SiO_2 sépare la ligne signal du niveau RDL du substrat. La structure se présente donc telle qu'illustrée en Figure B-40.

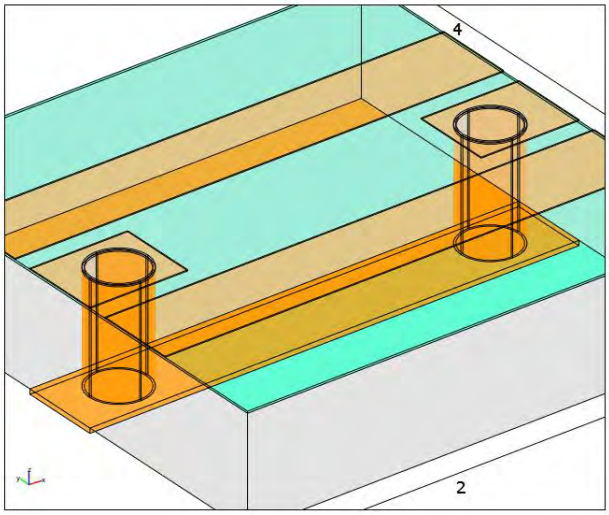


Figure B-40 Structure en « U »: d'une ligne signal située au niveau RDL + 2 TSV + 2 lignes de masse localisées au niveau BEOL.

Les TSVs sont de forme conique et réalisés en cuivre. Des éléments série (inductances partielles et résistances) modélisent la propagation du signal au travers du TSV. Les éléments parallèles servent quant à eux à modéliser les interactions entre le TSV et leur environnement. Les courants se propagent verticalement de la couche d'épitaxie aux lignes de masse. Ce chemin est modélisé par une résistance en parallèle avec une capacité auxquelles s'ajoutent en série la capacité de la mince couche d'oxyde séparant TSV et substrat et celle relative à la couche de SiO_2 séparant les lignes de masse du substrat. La présence d'une ligne de masse de part et d'autre des TSVs implique de modéliser deux chemins (Figure B-41).

Au final, cela revient pour le TSV à considérer une structure 4 ports. Deux servent à connecter les niveaux RDL et BEOL alors que les deux autres servent à traduire l'interaction existant entre le TSV et les deux lignes de masse du niveau BEOL. A noter que le TSV, modélisé ici sous ADS, est un sous-composant pouvant être inclus dans d'autres modèles (voir plus loin).

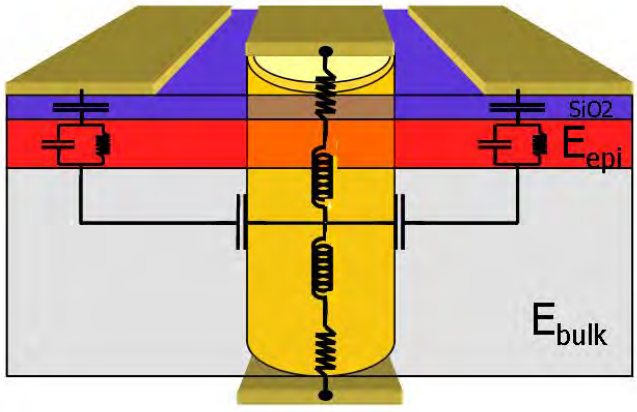


Figure B-41 Modèle RLCG du TSV. TSV + chemins des courants entre le TSV et les deux lignes de masse du niveau BEOL situées de part et d'autre du TSV.

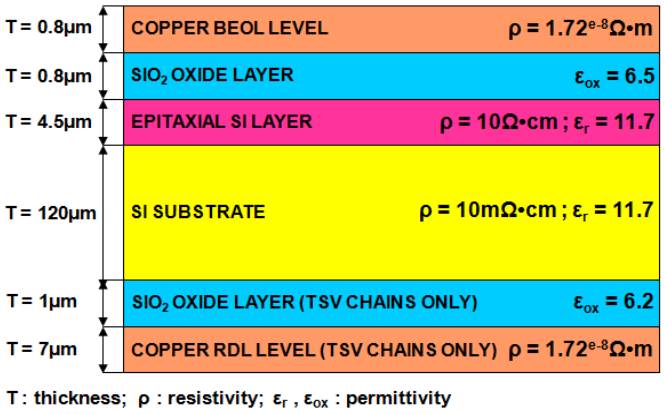


Figure B-42 Les données géométriques et technologiques des couches composées dans la CPW et structures de la chaîne TSV.

Les structures d'essai sont réalisées en utilisant un substrat de silicium hautement conducteur ayant une épaisseur de 120 microns, une résistivité ρ = mΩ•cm et une permittivité relative ε_r = 11,7. Sur le substrat est déposée une mince couche épitaxiale (épaisseur : 4,5µm, de résistivité: 10 Ω • cm, permittivité: 11,7). Les lignes au niveau BEOL, pour TSPE TSV et des chaînes, sont isolées du substrat par une couche d'oxyde (épaisseur : 0,8µm, de permittivité relative : 6,2). En ce qui concerne les chaînes de TSVs, une couche d'oxyde (épaisseur : 1µm, de permittivité : 6,5) est ajoutée à l'arrière de la structure pour isoler la ligne BRDL du substrat. Toutes les couches utilisées pour le PTC et des structures de chaîne TSV sont représentées sur la Figure B-42 avec leurs caractéristiques respectives. Les tronçons de ligne de niveau BEOL ont une épaisseur de 0,8µm, et 7µm pour le niveau RDL.

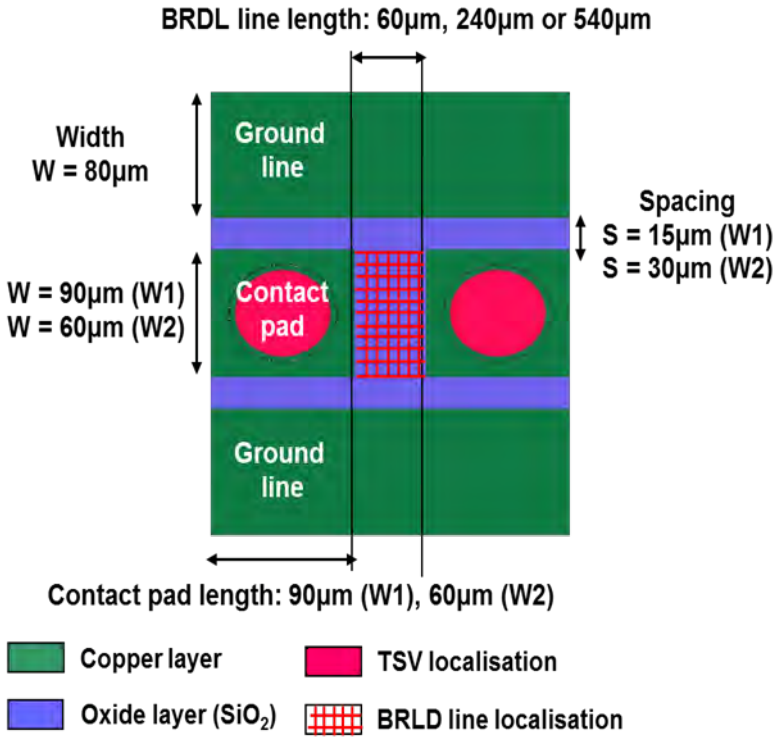


Figure B-43 Vue de dessus d'une configuration de structure de la chaîne 2xTSV

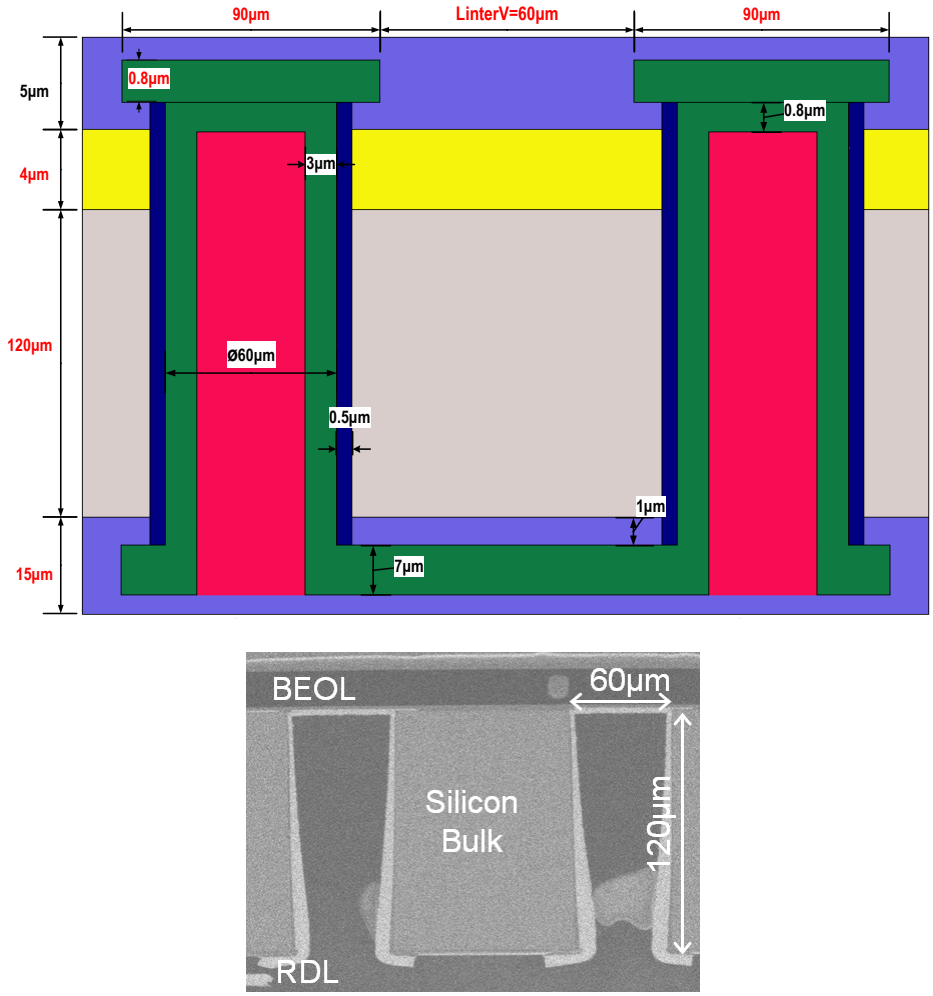


Figure B-44 SEM section transversale du TSV densité moyenne utilisé dans les chaînes TSV (configuration W1)

Pour les chaînes TSV, la longueur de la ligne BRDL peut avoir l'une des trois valeurs: 60µm, 240µm et 540µm. Comme pour les TSPE, il existe deux configurations pour la chaîne TSV. Dans la configuration W1, la largeur de la ligne BRDL et des plots de contact sont de 90 µm (60 microns pour W2). La distance séparant les plages de contact et les lignes de masse dépend aussi de la configuration. Les valeurs de l'écartement sont identiques à celles pour les structures de CPW; comme le sont les largeurs de ligne de base. La Figure B-43 montre la vue de dessus de la chaîne 2xTSV et la Figure B-44 représente la vue en coupe. Par souci de clarté, la ligne BRDL et les localisations des plots de contact y sont indiquées.

Les différentes couleurs représentent différents matériaux, comme dans tableau souvent.

Color	*Material*	*Physics property*	*Description*
	Copper	σ=5e7S/m	M1 and the TSV
	SiO_2	ε_r=6.6	Top Oxide layer and back Oxide layer
	SiO_2	ε_r=6.5	Surface of TSV called sidewall SiO2
	Si Epitaxial	σ=10S/m ε_r=11.7	Epitaxial layer
	Silicon	σ=10^4S/m ε_r=11.7	Silicon bulk
	SINR	ε_r=3.4	Filling TSV

La caractérisation de l'interconnexion est définie comme un modèle électrique équivalent à extraire de mesures. Par exemple, on extrait en fonction de la fréquence, l'impédance caractéristique et un exposant de propagation ou des éléments distribués R, L, C et G du modèle équivalent de l'équation des télégraphes et à partir de la mesure de la matrice de diffusion -S(cattering)- de cette interconnexion à l'aide d'un analyseur de vectoriel de réseau (VNA). Dans la pratique, cette interconnexion qui peut être appelée dispositif sous test (DUT), est généralement dans un environnement de test complexe ; il ne permet pas à l'expérimentateur d'extraire ses paramètres par une seule mesure. En fait, cette interconnexion est enterrée dans une cellule pour se connecter au système de mesure (dans le cas général, nous trouvons la présence de plots de contact, des sections d'accès, de câbles, de lignes de connexion ....). Les méthodes «de-embedding» (désenrobage, épluchage) sont utilisées pour éviter l'influence de l'environnement et obtenir les caractéristiques intrinsèques du DUT pour nous, l'interconnexion.

Donc, l'approche de modélisation repose alors sur l'analyse des structures de test au moyen d'un outil électromagnétique 3D à l'aide de la méthode des éléments finis (FEM) [104] pour comprendre les phénomènes physiques et électriques qui se produisent en 3D, quant aux interconnexions, lors de la propagation du signal, et enfin sur l'utilisation d'une méthode de ligne de transmission.

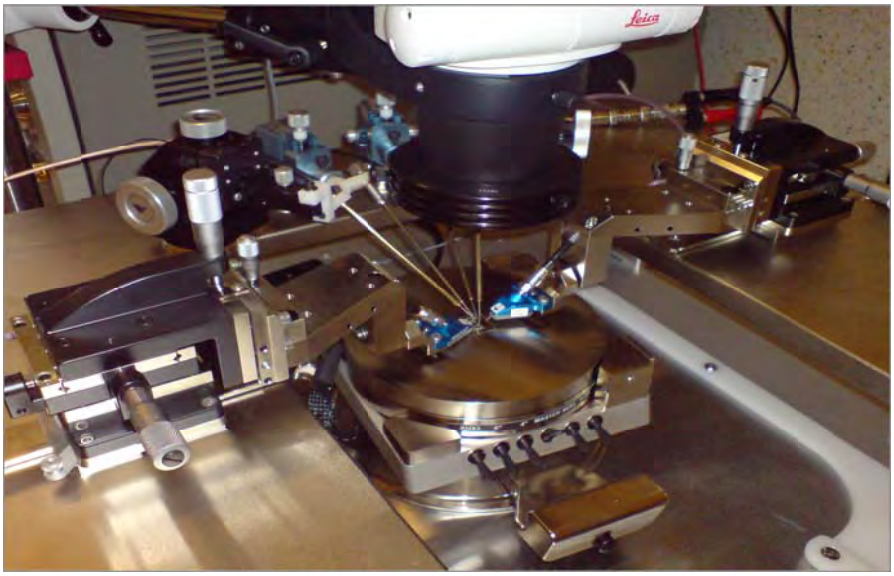


Figure B-45 Les mesures avec un analyseur de réseau vectoriel (VNA).

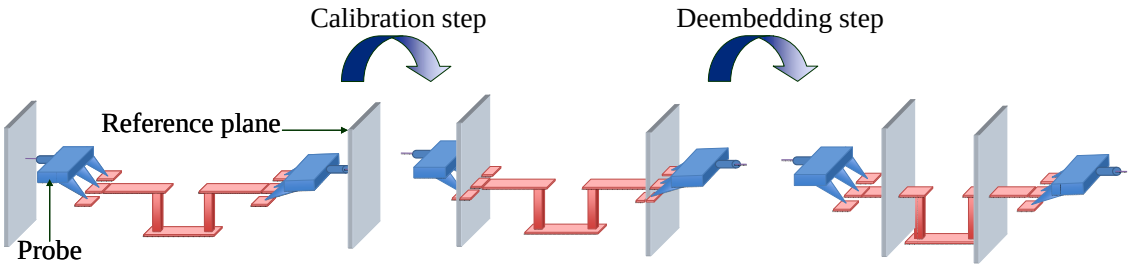


Figure B-46 Effets de la calibration et dé-enrobage

B.4.3. Simulation par elements finis

La simulation COMSOL est basée sur le module « fréquence radio ». Une différence majeure entre la modélisation quasi-statique et à haute fréquence est que les formulations

dépendent de la « taille électrique » de la structure. Cette mesure, sans dimension, est le rapport entre les plus grandes distances entre deux points de la structure, divisé par la longueur d'onde des champs électromagnétiques. Pour les simulations de structures ayant une dimension électrique dans la gamme jusqu'à 1/10 les formulations quasi-statiques sont appropriées. [141] L'hypothèse physique de ces situations est que les retards de la propagation des ondes sont suffisamment petits pour être négligés et . Ainsi, des déphasages ou des gradients de phase dans les champs sont causés par des matériaux et / ou par des couplages de conducteurs, inductifs ou capacitifs, plutôt que d'être provoqué par des retards de propagation. Pour électromagnétisme électrostatique, magnétostatique, en quasi-statique, on utilise le module AC / DC, un module multi-physique de COMSOL complémentaire de électromagnétisme basse fréquence. Lorsque des retards de propagation deviennent importants, il est nécessaire d'utiliser les équations de Maxwell complètes pour les ondes électromagnétiques à haute fréquence : le module « full wave » (que nous n'avons encore pas). Elles sont appropriées pour les structures de taille électrique 1/100 et plus. Ainsi, une zone de chevauchement existe où l'on peut utiliser à la fois le plein des interfaces quasi-statique et physique Maxwell.

Nous fixons la limite de la surface extérieure avec les "Scattering Boundary Conditions ".

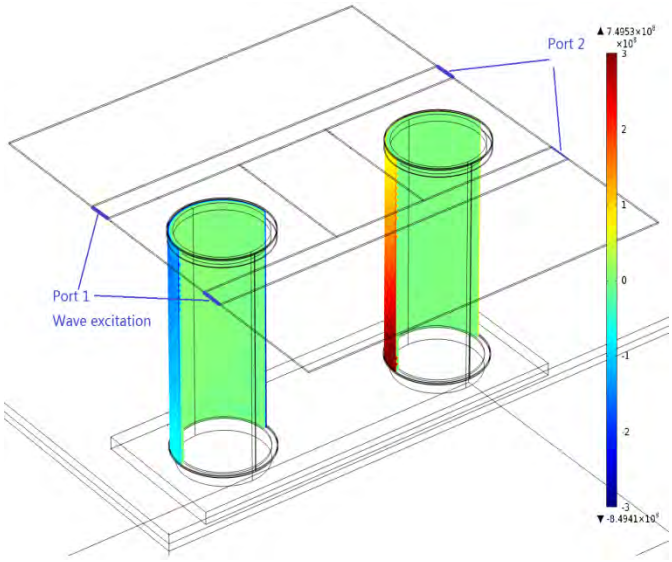


Figure B-47 Ports localisés (Lumped Ports)

Les ports localisés (lumped) sont fixés comme indiqué sur l'image ci-dessus (Figure B-47). L'impédance caractéristique est de 50Ω pour chaque port.

Les tailles et la forme des mailles jouent un rôle très important dans la simulation par éléments finis. Un maillage optimal conduit à des résultats précis avec moins de temps et la consommation de mémoire. Outre le maillage de contrôle physique, le maillage manuel peut également être utilisé. Un maillage viable pourrait être créé par la technologie de maillage balayé et la technologie de maillage en couches [143]. Le maillage peut être comme sur la figure suivante.

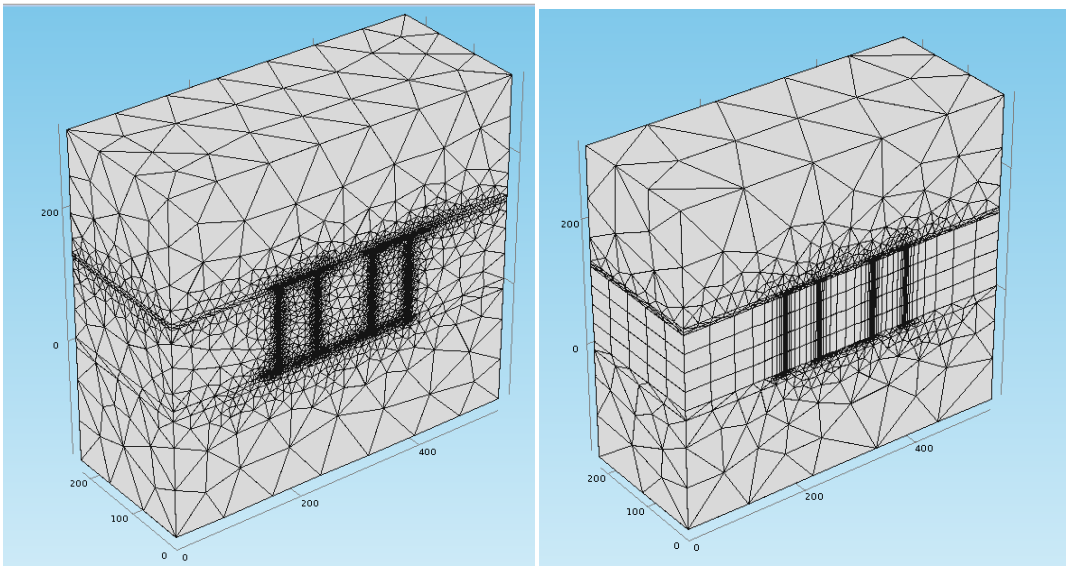


Figure B-48 Contrôle physique des mailles (à gauche) et l'utilisation manuelle de maille Swept Mesh Tech (à droite).

S'intéressant à l' "Effet peau" sur la surface extérieure du TSV, un « Layered Mesh » idoine pourrait être utilisé sur la surface du TSV afin d'améliorer la précision du résultat. Ce maillage des couches pourrait produire une maille très fine sur le domaine « proche de la surface ».

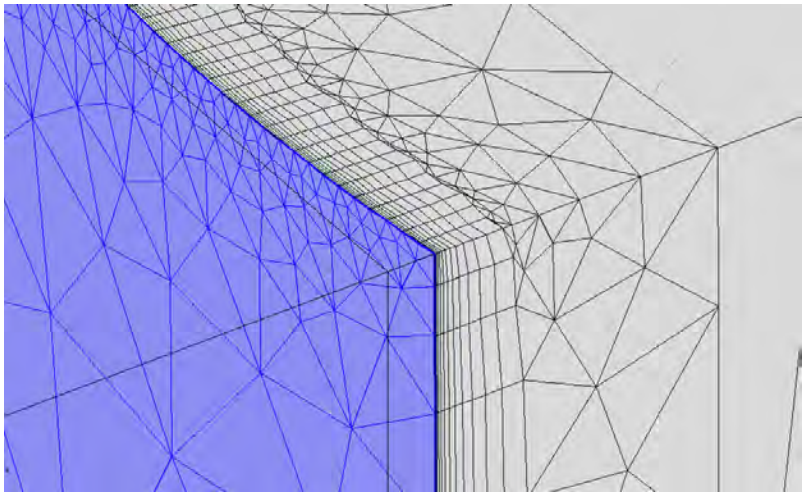


Figure B-49 Couches maillées sur la surface de TSV

B.4.4. Résultats de test et de modèles compacts

Pour la première structure (cf. Figure B-39), les résultats de l'expérience et ADS simulations de paramètres S sont présentés dans la Figure B-50. Les lignes bleues sont les résultats de l'expérience et les rouges sont les résultats de la simulation 3D-TLE/ADS.

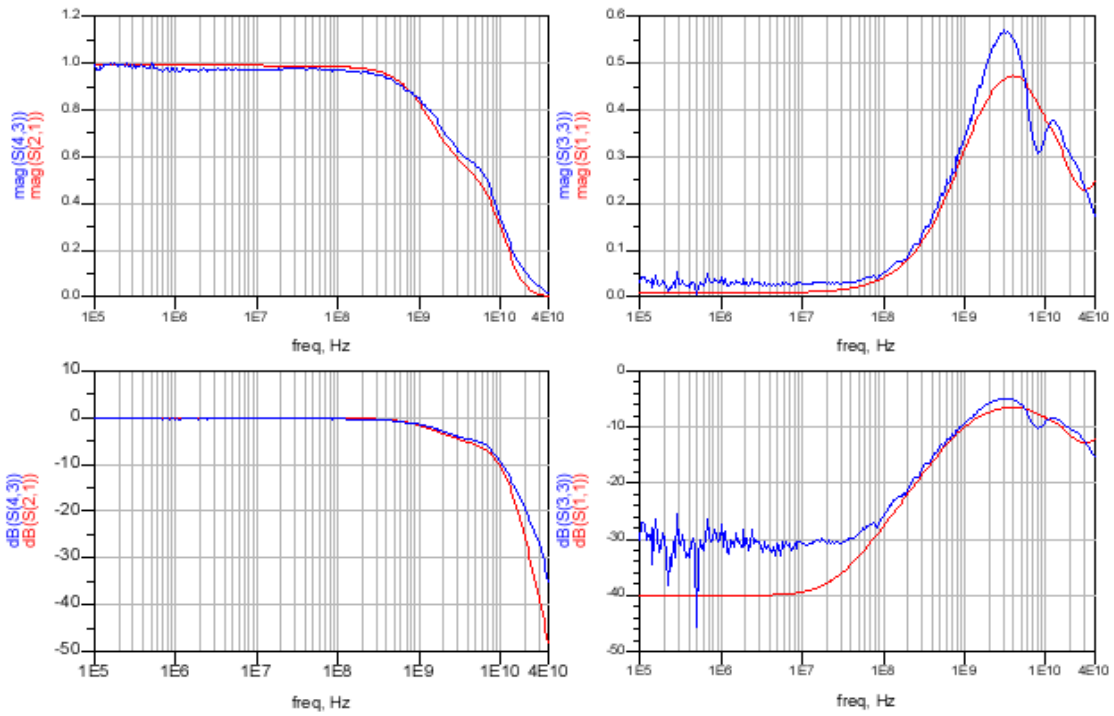


Figure B-50 S parameter for the simple CPW structure (S21 left; S11 right)

Nous utilisons l'optimisation des ADS, qui tente d'avoir le "meilleur" série de paramètre, la différence au bout d'environ 5 GHz fréquence est causée par les paramètres dépendent de la fréquence (capacité de paramètre à haute fréquence, effet de peau), puis nous devons affiner notre modèle au-delà de la fréquence 5GHz.

La distribution du potentiel de cette structure est également étudiée sous COMSOL. La Figure B-51donne la distribution de potentiel sur et en dessous de la couche d'oxyde, respectivement.

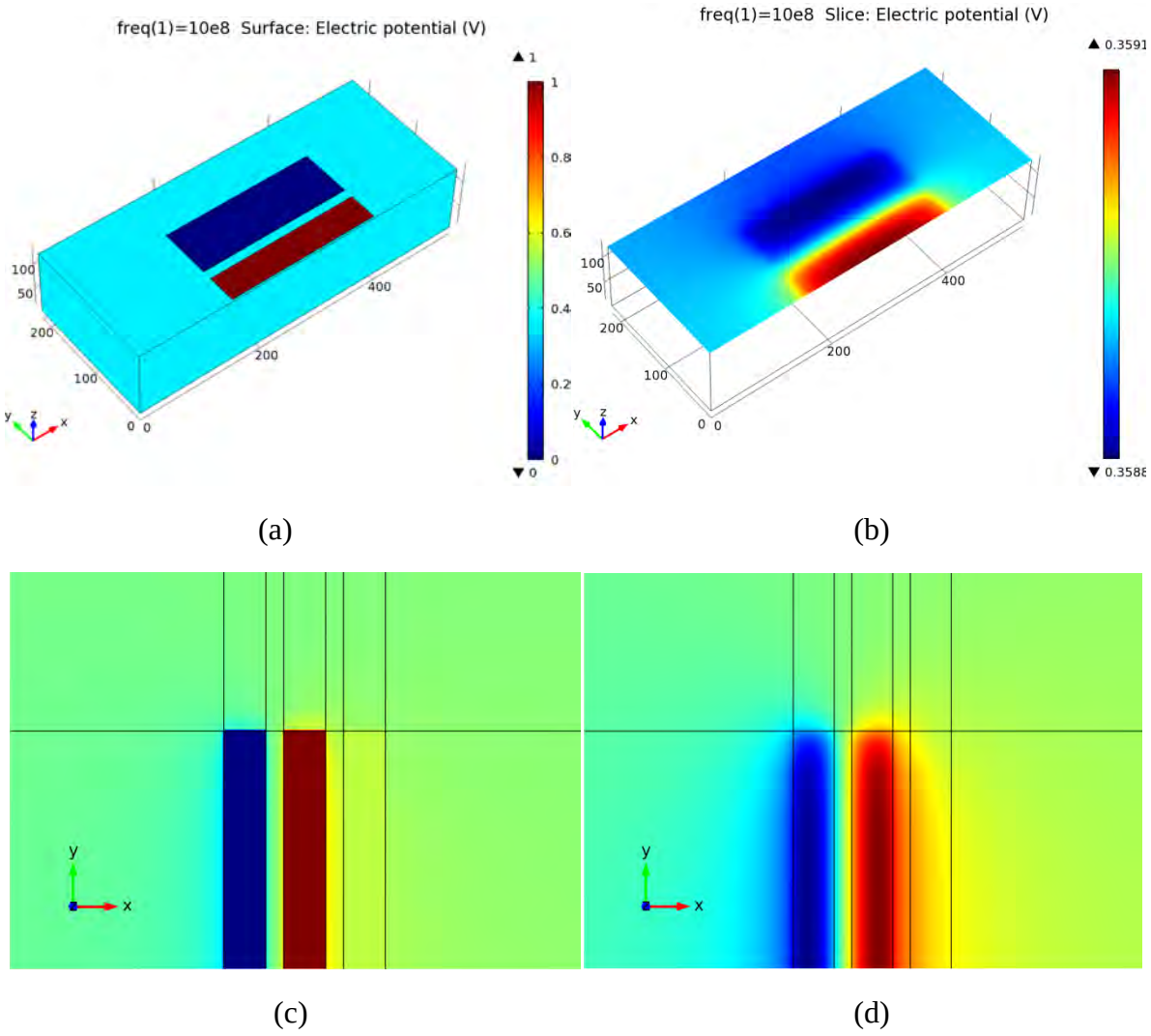


Figure B-51 Potential distribution upon the oxide layer (a) (c) and below the oxide layer (b) (d) (from COMSOL)

D'après le résultat on peut trouver, bien que le potentiel sur la couche d'oxyde soit uniforme, le potentiel sous la couche d'oxyde (c'est à dire sur le dessus du substrat) n'est pas uniforme. C'est pourquoi nous n'utilisons pas une tension constante sur le calcul de l'impédance du substrat au chapitre 3.

A potential distribution below the oxide layer calculated from 3D-IE for the same structure is showed as followed (Figure B-52).

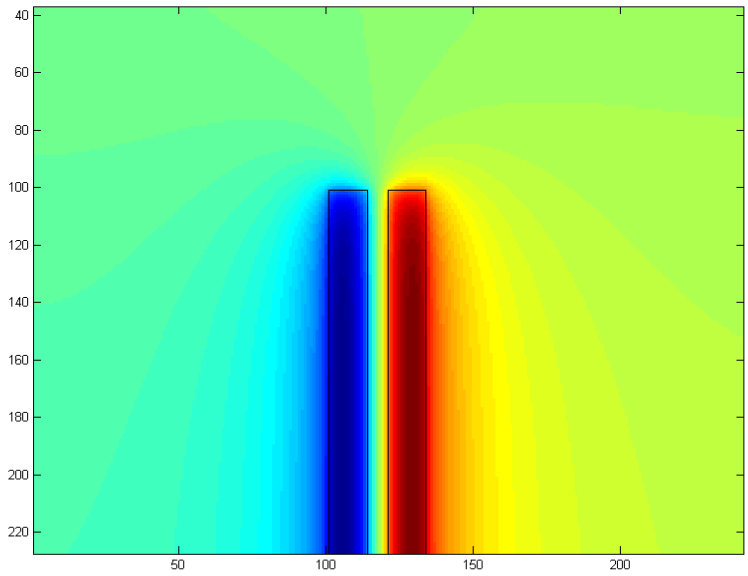


Figure B-52 Potential distribution below the oxide layer from 3D-IE

Comparer Figure B-52 avec la Figure B-51 (b) et (d), nous pouvons trouver le résultat 3D-IE est bien correspondant au résultat COMSOL. Et cela prouve aussi l'utilisation de la méthode de courant constant est plus précise que la méthode de tension constante sur le dessus du substrat.

Les résultats des comparaisons sont présentés sur la Figure B-53. Les réponses en RF des structures de test sont tracées avec des courbes rouges continuees - celles des modèles électriques-, et avec des courbes bleues pointillées- les mesures réseau-. Les modèles RLCG compacts équivalents proposés pour les guides d'ondes coplanaires et les chaînes TSV montrent une très bonne précision pour des fréquences allant jusqu'à 20 GHz et 10 GHz, respectivement. Certains pics peuvent être observés dans les mesures, mais pas dans les simulations à « basse » fréquence (en dessous de 1 GHz). Ces résonances sont dues au couplage entre le substrat de la structure de test et de son environnement de mesure.

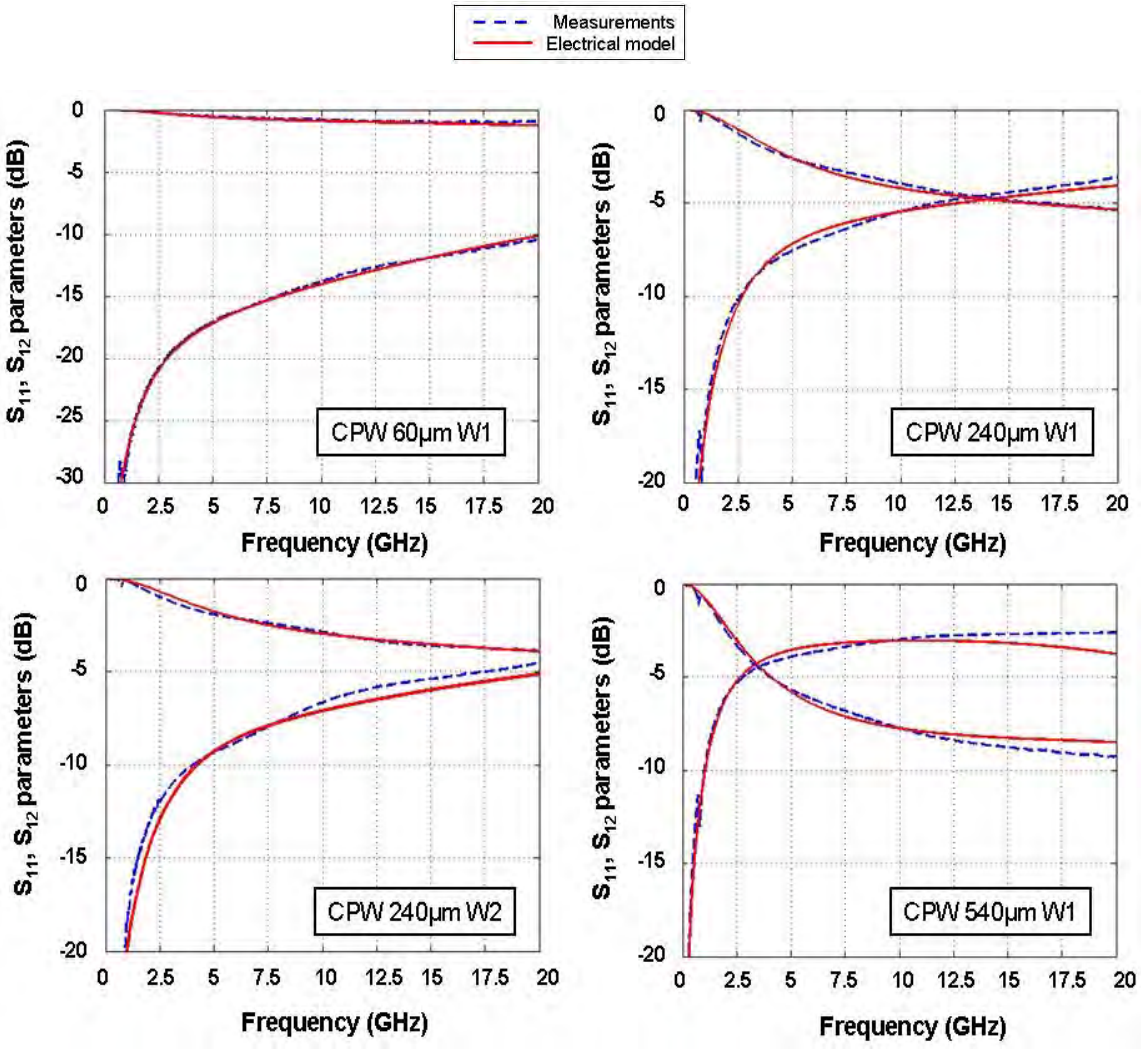


Figure B-53 Comparaison de paramètres S, jusqu'à 20 GHz, entre les mesures effectuées sur des structures de test de guides d'ondes coplanaires et les simulations de leurs modèles équivalents électriques pour à la fois W1 et W2 et des configurations de différentes longueurs de lignes coplanaires.

Les guides d'ondes coplanaires de configuration W2 donnent lieu à une meilleure transmission résultant de pertes d'insertion dues à une impédance plus élevée le long du chemin de fuite à travers le substrat. La largeur de la ligne de signal est plus faible dans cette configuration, résultant en une capacité d'oxyde inférieure. Néanmoins, les pertes d'insertion sont dominées par les lignes BEOL: pertes résistives coplanaires qui augmentent pour des longueurs de ligne supérieures.

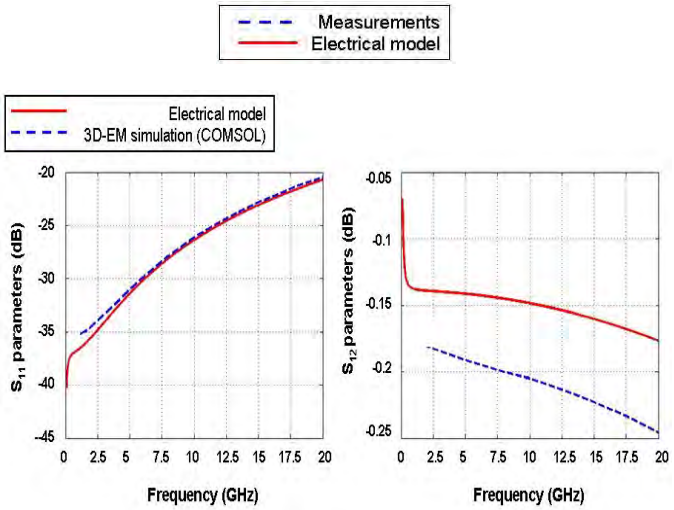


Figure B-54 Comparaison des paramètres S pour un système de guide d'ondes 240 μm coplanaire au sommet d'un substrat fortement résistif. Le substrat est modélisé avec des paramètres électriques DC. Gauche: paramètres S_{11}. A droite: paramètres S_{12}

A très haute fréquence, l'erreur d'estimation entre les réponses RF des structures de test et celles de leurs modèles électriques équivalents est supérieure à 10% en raison des effets de couplage de substrat négligés. La méthode d'extraction du substrat, associée à l'approche de modélisation, est validée ici pour un guide d'ondes coplanaire au sommet d'un substrat fortement résistif. Les paramètres S proposés par le modèle électrique ont été comparés, pour une plage de fréquences allant jusqu'à 20 GHz avec des réponses obtenues à partir d'une simulation de la structure réalisée sous un simulateur électromagnétique FEM 3D [104]. Les résultats de cette comparaison sont présentés sur la Figure B-54. Le pourcentage d'erreur dans l'évaluation de S_{12} est relativement élevé alors que les pertes sont en fait pratiquement négligeables, comme on peut le voir sur la figure.

B.5 Perspectives et futures directions

Les prospectives et l'avenir sont ici introduits. C'est d'abord l'étude de l'intégrité du signal dans des matrices TSV. Ensuite, l'analyse (electro-)thermique de la structure TSV est notée. L'effet de peau - dernier chapitre -, et les courants de Foucault au niveau du TSV devraient être également analysés. Un début de résultat sur la possible corrélation de fluctuations de signaux, en deux points distincts en volume, est présentée ; ceci devraient initier l'étude des corrélations de sources de bruit, dans les circuits 3D, en particulier à l « échelle nanométrique ». Nous finissons par une conclusion de ce chapitre.

Des analyses temporelles sont présentées ici: diagrammes de l'œil réalisés sur différentes configurations de matrice TSV, selon les types de signaux envoyés au TSV près des extrémités, pour étudier les problèmes d'intégrité du signal dans de telles structures 3D. Les résultats montrent que l'extracteur 3D TLE peut être facilement intégré à un environnement commun EDA en fournissant des modèles compacts capables, par exemple, d'analyser la performance des faisceaux TSV pour la communication de données à haute vitesse.

En 3D, les dispositifs de dissipation de chaleur ont, a priori, une densité de chaleur plus élevée que dans une puce 2D comparable quant aux fonctionnalités. La Figure B-55 montre par exemple, une carte de température dans une SRAM (calculs FEM).

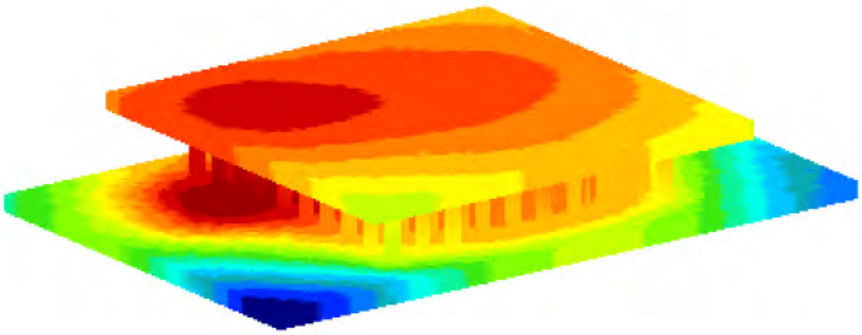


Figure B-55 Carte de température dans une SRAM [147]

Reference

[1] J. H. Lau, *Advanced MEMS packaging*: McGraw-Hill, 2010.

[2] J. H. Lau, *Reliability of rohs-compliant 2d and 3d ic interconnects*: McGraw-Hill, 2011.

[3] G. E. Moore, "Cramming more components onto integrated circuits," ed: McGraw-Hill, 1965.

[4] J. H. Lau, "Evolution and outlook of TSV and 3D IC/Si integration," in *Electronics Packaging Technology Conference (EPTC), 2010 12th*, 2010, pp. 560.

[5] R. S. Patti, "Three-dimensional integrated circuits and the future of system-on-chip designs," *Proceedings of the IEEE,* vol. 94, pp. 1214, 2006.

[6] K. L. Tai, "System-In-Package (SIP): challenges and opportunities," in *Proceedings of the 2000 Asia and South Pacific Design Automation Conference*, 2000, pp. 191.

[7] R. Weerasekera, "System Interconnection Design Trade-offs in Three-Dimensional (3-D) Integrated Circuits," KTH, 2008.

[8] J. Kim and J. Cho, "TSV modeling and noise coupling in 3D IC," presented at the Electronic System-Integration Technology Conference (ESTC), 2010 3rd, Berlin, 2010.

[9] D. H. Kim, S. Mukhopadhyay, and S. K. Lim, "Fast and accurate analytical modeling of through-silicon-via capacitive coupling," *Components, Packaging and Manufacturing Technology, IEEE Transactions on,* pp. 0, 2011.

[10] J. H. Lau, "The Most Cost-Effective Integrator (TSV Interposer) for 3D IC Integration System-in-Package (SiP)," 2011.

[11] V. F. Pavlidis and E. G. Friedman, *Three-dimensional integrated circuit design*: Morgan Kaufmann, 2010.

[12] T. Yoshinaga and M. Nomura, "Trends in R&D in TSV technology for 3D LSI packaging," *Science & Technology Trends, Quarterly Rev,* vol. 37, p. 26, 2010.

[13] W. R. Davis, J. Wilson, S. Mick, J. Xu, H. Hao, C. Mineo, A. M. Sule, M. Steer, and P. D. Franzon, "Demystifying 3D ICs: the pros and cons of going vertical," *Design & Test of Computers, IEEE,* vol. 22, pp. 498, 2005.

[14] Renesas. Available: http://www.renesas.eu/

[15] J. H. Lau, "Who Invented the TSV and When?," in *Who Invented the TSV and When?*, ed: 3D InCites, 2010.

[16] W. Shockley, "Semiconductive Wafer and Method of Making the Same," US Patent # 3,044,909, 1958.

[17]J. U. Knickerbocker, P. S. Andry, B. Dang, R. R. Horton, M. J. Interrante, C. S. Patel, R. J. Polastre, K. Sakuma, R. Sirdeshmukh, E. J. Sprogis, C. K. Tsang, B. C. Webb, and S. L. Wright, "Three-dimensional silicon integration," *IBM Journal of Research and Development,* vol. 52, pp. 553, 2008.

[18] J. H. Lau and X. Zhang, "Effects of TSV Interposer on the Reliability of 3D IC Integration SiP," *ASME Paper no. InterPACK2011-52205,* 2011.

[19] A. Sheibanyrad, *3D Integration for NoC-based SoC Architectures*: Springer Science+ Business Media, 2011.

[20] J.-M. Yannou, "Present and future of 3D integration," in *MINATEC Crossroads*, Grenoble, France, 2010.

[21] J. T. Pawlowski, "Hybrid memory cube: breakthrough DRAM performance with a fundamentally re-architected DRAM subsystem," in *Proceedings of the 23rd Hot Chips Symposium*, 2011.

[22] J. T. Pawlowski, "Hybrid Memory Cube (HMC)," in *Proceedings of Hot Chips*, 2011.

[23] J. Jeddeloh and B. Keeth, "Hybrid memory cube new DRAM architecture increases density and performance," in *VLSI Technology (VLSIT), 2012 Symposium on*, 2012, pp. 87.

[24] HMC. Available: http://www.hybridmemorycube.org/

[25] I. Limansyah, M. Wolf, A. Klumpp, K. Zoschke, R. Wieland, M. Klein, H. Oppermann, L. Nebrich, A. Heinig, and A. Pechlaner, "3d image sensor sip with tsv

silicon interposer," in *Electronic Components and T echnology Conference, 2009. ECTC 2009. 59th*, 2009, pp. 1430.

[26] M. Motoyoshi and M. Koyanagi, "3D-LSI technology for image sensor," *Journal of Instrumentation,* vol. 4, p. P03009, 2009.

[27]I. Limansyah, M. J. Wolf, A. Klumpp, K. Zoschke, R. Wieland, M. Klein, H. Oppermann, L. Nebrich, A. Heinig, A. Pechlaner, H. Reichl, and W. Weber, "3D image sensor SiP with TSV silicon interposer," in *Electronic Components and Technology Conference, 2009. ECTC 2009. 59th*, 2009, pp. 1430.

[28] M. J. Wolf, K. Zoschke, A. Klumpp, R. Wieland, M. Klein, L. Nebrich, A. Heinig, I. Limansyah, W. Weber, O. Ehrmann, and H. Reichl, "3D integration of image sensor SiP using TSV silicon interposer," in *Electronics Packaging Technology Conference, 2009. EPTC '09. 11th*, 2009, pp. 795.

[29] J. Charbonnier, D. Henry, F. Jacquet, B. Aventurier, C. Brunet-Manquat, G. Enyedi, N. Bouzaida, V. Lapras, and N. Sillon, "Wafer level packaging technology development for CMOS image sensors using Through Silicon Vias," in *Electronics System-Integration Technology Conference, 2008. ESTC 2008. 2nd*, 2008, pp. 141.

[30] P. Viaud, "3D TSV Market Trends," in *SÜSS Asia Technology Forum*, China, 2012.

[31] R. Weidlich, "What comes Next in Commodity DRAMS—DDR3," *Infineon Technologies, Jun,* 2005.

[32] P. Ramm, A. Klumpp, J. Weber, and M. M. Taklo, "3D System-on-Chip technologies for More than Moore systems," *Microsystem technologies,* vol. 16, pp. 1051, 2010.

[33] A. Wilson, "Wafer-scale manufacturing techniques are reducing the size and cost of color cameras," *Vision Systems Design,* 2010.

[34] Y. Liang and Y. Li, "Closed-form expressions for the resistance and the inductance of different profiles of through-silicon vias," *Electron Device Letters, IEEE,* vol. 32, pp. 393, 2011.

[35] C. Li, W.-j. Zhang, and Z.-p. Yu, "Multi-Layered Green Function Approach to 3D Capacitance Extraction," *Microelectronics,* vol. 35, 2005.

[36] D. H. Kim, S. Mukhopadhyay, and S. K. Lim, "Fast and accurate analytical modeling of through-silicon-via capacitive coupling," *Components, Packaging and Manufacturing Technology, IEEE Transactions on,* vol. 1, pp. 168, 2011.

[37] Y. Eo and W. R. Eisenstadt, "High-speed VLSI interconnect modeling based on S-parameter measurements," *Components, Hybrids, and M anufacturing Technology, IEEE Transactions on,* vol. 16, pp. 555, 1993.

[38] P. S. Crovetti and F. L. Fiori, "Efficient BEM-based substrate network extraction in silicon SoCs," *Microelectronics Journal,* vol. 39, pp. 1774, 2008.

[39] O. Valorge, F. Calmon, C. Andrei, C. Gontrand, and P. Dautriche, "Mixed-signal IC design guide to enhance substrate noise immunity in bulk silicon technology," *Analog Integrated Circuits and S ignal Processing,* vol. 63, pp. 185, 2010.

[40] Z. Xu and J.-Q. Lu, "High-speed design and broadband modeling of through-strata-vias (TSVs) in 3D integration," *Components, Packaging and Manufacturing Technology, IEEE Transactions on,* vol. 1, pp. 154, 2011.

[41] I. Savidis and E. G. Friedman, "Closed-form expressions of 3-D via resistance, inductance, and capacitance," *Electron Devices, IEEE Transactions on,* vol. 56, pp. 1873, 2009.

[42] W. R. Davis, J. Wilson, S. Mick, J. Xu, H. Hua, C. Mineo, A. M. Sule, M. Steer, and P. D. Franzon, "Demystifying 3D ICs: the pros and cons of going vertical," *Design & Test of Computers, IEEE,* vol. 22, pp. 498, 2005.

[43] G. Poupon, N. Sillon, D. Henry, C. Gillot, A. Mathewson, L. Di Cioccio, B. Charlet, P. Leduc, M. Vinet, and P. Batude, "System on wafer: a new silicon concept in sip," *Proceedings of the IEEE,* vol. 97, pp. 60, 2009.

[44] Y. Akasaka, "Three-dimensional IC trends," *Proceedings of the IEEE,* vol. 74, pp. 1703, 1986.

[45] T. Fukushima, H. Kikuchi, Y. Yamada, T. Konno, J. Liang, K. Sasaki, K. Inamura, T. Tanaka, and M. Koyanagi, "New three-dimensional integration technology based on reconfigured wafer-on-wafer bonding technique," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, 2007, pp. 985.

[46] K. Sakuma, P. Andry, C. Tsang, K. Sueoka, Y. Oyama, C. Patel, B. Dang, S. Wright, B. Webb, and E. Sprogis, "Characterization of stacked die using die-to-wafer integration for high yield and throughput," in *Electronic Components and Technology Conference, 2008. ECTC 2008. 58th*, 2008, pp. 18.

[47] J. Lau, "State-of-the-art and trends in 3D integration," *Chip Scale Review,* pp. 22, 2010.

[48] T.-Y. Wang, J.-L. Tsai, and C. C.-P. Chen, "Thermal and power integrity based power/ground networks optimization," in *Proceedings of the conference on Design, automation and test in Europe-Volume 2*, 2004, p. 20830.

[49] S. Im and K. Banerjee, "Full chip thermal analysis of planar (2-D) and vertically integrated (3-D) high performance ICs," in *Electron Devices Meeting, 2000. IEDM'00. Technical Digest. International*, 2000, pp. 727.

[50] K. Banerjee, M. Pedram, and A. H. Ajami, "Analysis and optimization of thermal issues in high-performance VLSI," in *Proceedings of the 2001 international symposium on Physical design*, 2001, pp. 230.

[51] A. Jain, R. E. Jones, R. Chatterjee, and S. Pozder, "Analytical and numerical modeling of the thermal performance of three-dimensional integrated circuits," *Components and Packaging Technologies, IEEE Transactions on,* vol. 33, pp. 56, 2010.

[52] M. Lee, J. Cho, J. Kim, J. S. Pak, J. Kim, H. Lee, J. Lee, and K. Park, "Temperature-dependent through-silicon via (TSV) model and noise coupling," in *Electrical Performance of Electronic Packaging and Systems (EPEPS), 2011 IEEE 20th Conference on*, 2011, pp. 247.

[53] C. S. Selvanayagam, J. H. Lau, X. Zhang, S. Seah, K. Vaidyanathan, and T. Chai, "Nonlinear thermal stress/strain analyses of copper filled TSV (through silicon via) and their flip-chip microbumps," *Advanced Packaging, IEEE Transactions on,* vol. 32, pp. 720, 2009.

[54] S. K. Ryu, T. Jiang, K. H. Lu, J. Im, H. Y. Son, K. Y. Byun, R. Huang, and P. S. Ho, "Characterization of thermal stresses in through-silicon vias for three-dimensional interconnects by bending beam technique," *Applied Physics Letters,* vol. 100, pp. 041901, 2012.

[55] G. Y. Huang and C. M. Tan, "Electrical-Thermal-Stress Coupled-field Effect in SOI and Partial SOI Lateral Power Diode," *Power Electronics, IEEE Transactions on,* pp. 1, 2011.

[56] S. Park, H. Bang, H. Bang, and J. You, "Thermo-mechanical analysis of TSV and solder interconnects for different Cu pillar bump types," *Microelectronic Engineering,* vol. 99, pp. 38, 2012.

[57] J. Zhang, M. O. Bloomfield, J.-Q. Lu, R. J. Gutmann, and T. S. Cale, "Modeling thermal stresses in 3-D IC interwafer interconnects," *Semiconductor Manufacturing, IEEE Transactions on,* vol. 19, pp. 437, 2006.

[58] S. Grivet-Talocia, I. Stievano, I. Maio, and F. Canavero, "Combined FDTD/Macromodel simulation of interconnected digital devices," in *Proceedings of the conference on Design, Automation and Test in Europe-Volume 1*, 2003, p. 10536.

[59] CATRENE. Available: http://www.catrene.org/

[60] CATRENE. 3D-TSV integration for multimedia and mobile applications (3DIM3) [Online]. Available: http://www.catrene.org/web/downloads/profiles_catrene/CT105-3DIM3-project%20profile-final%20(7-6-11).pdf

[61] P. Leduca, F. de Crecy, M. Fayolle, B. Charlet, T. Enot, M. Zussy, B. Jones, J.-C. Barbe, N. Kernevez, and N. Sillon, "Challenges for 3D IC integration: bonding quality and thermal management," in *International Interconnect Technology Conference, IEEE 2007*, 2007, pp. 210.

[62] S. Onkaraiah and C. S. Tan, "Mitigating heat dissipation and thermo-mechanical stress challenges in 3-D IC using thermal through silicon via (TTSV)," in *Electronic Components and T echnology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 411.

[63] C. Okoro, R. Agarwal, P. Limaye, B. Vandevelde, D. Vandepitte, and E. Beyne, "Insertion bonding: A novel Cu-Cu bonding approach for 3D integration," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 1370.

[64] E. Higurashi, D. Chino, T. Suga, and R. Sawada, "Au–Au Surface-Activated Bonding and Its Application to Optical Microsensors With 3-D Structure," *Selected Topics in Quantum Electronics, IEEE Journal of,* vol. 15, pp. 1500, 2009.

[65] N. H. Khan, S. M. Alam, and S. Hassoun, "Through-silicon via (TSV)-induced noise characterization and noise mitigation using coaxial TSVs," in *3D System Integration, 2009. 3DIC 2009. IEEE International Conference on*, 2009, pp. 1.

[66] L. Cadix, C. Bermond, C. Fuchs, A. Farcy, P. Leduc, L. DiCioccio, M. Assous, M. Rousseau, F. Lorut, and L. Chapelon, "RF characterization and modelling of high density Through Silicon Vias for 3D chip stacking," *Microelectronic Engineering,* vol. 87, pp. 491, 2010.

[67] D. Archard, K. Giles, A. Price, S. Burgess, and K. Buchanan, "Low temperature PECVD of dielectric films for TSV applications," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 764.

[68] H.-s. Noh, K.-s. Moon, A. Cannon, P. J. Hesketh, and C. Wong, "Wafer bonding using microwave heating of parylene intermediate layers," *Journal of Micromechanics and Microengineering,* vol. 14, p. 625, 2004.

[69] K. Fujimoto, N. Maeda, H. Kitada, Y. Kim, A. Kawai, K. Arai, T. Nakamura, K. Suzuki, and T. Ohba, "Development of multi-stack process on wafer-on-wafer (WOW)," in *CPMT Symposium Japan, 2010 IEEE*, 2010, pp. 1.

[70] I.-S. Kang, G.-J. Jung, B.-Y. Jeon, J.-H. Yoo, and S.-H. Jeong, "Wafer level embedded System in Package (WL-eSiP) for mobile applications," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 309.

[71] K. Zoschke, M. Wegner, M. Wilke, N. Jurgensen, C. Lopper, I. Kuna, V. Glaw, J. Roder, O. Wunsch, and M. Wolf, "Evaluation of thin wafer processing using a temporary wafer handling system as key technology for 3D system integration," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 1385.

[72] X. Pang, T. Chua, H. Li, E. Liao, W. Lee, and F. Che, "Characterization and management of wafer stress for various pattern Densities in 3D integration technology," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 1866.

[73] A. C. Fischer, "Integration and Fabrication Techniques for 3D Micro-and Nanodevices," Karlstad University, 2012.

[74] K. Au, S. Kriangsak, X. Zhang, W. Zhu, and C. Toh, "3D chip stacking & reliability using TSV-micro C4 solder interconnection," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 1376.

[75] M. Sekiguchi, H. Numata, N. Sato, T. Shirakawa, M. Matsuo, H. Yoshikawa, M. Yanagida, H. Nakayoshi, and K. Takahashi, "Novel low cost integration of through chip interconnection and application to CMOS image sensor," in *Electronic Components and Technology Conference, 2006. Proceedings. 56th*, 2006, p. 8 pp.

[76] J. D. Reed, M. Lueck, C. Gregory, A. Huffman, J. M. Lannon, and D. Temple, "High density interconnect at 10µm pitch with mechanically keyed Cu/Sn-Cu

and Cu-Cu bonding for 3-D integration," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 846.

[77] D. Lederer and J.-P. Raskin, "Substrate loss mechanisms for microstrip and CPW transmission lines on lossy silicon wafers," *Solid-State Electronics,* vol. 47, pp. 1927, 2003.

[78] M. Badaroglu, S. Donnay, H. De Man, Y. A. Zinzius, G. G. Gielen, W. Sansen, T. Fonden, and S. Signell, "Modeling and experimental verification of substrate noise generation in a 220-Kgates WLAN system-on-chip with multiple supplies," *Solid-State Circuits, IEEE Journal of,* vol. 38, pp. 1250, 2003.

[79] A. Koukab, K. Banerjee, and M. Declercq, "Modeling techniques and verification methodologies for substrate coupling effects in mixed-signal system-on-chip designs," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on,* vol. 23, pp. 823, 2004.

[80] N. Checka, "Substrate noise analysis and techniques for mitigation in mixed-signal RF systems," Massachusetts Institute of Technology, 2005.

[81] O. VALORGE, "Bruit d'Alimentation et Couplage par le Substrat dans les Circuits Mixtes," INSA-LYON, 2006.

[82] W. Jin, Y. Eo, J. Shim, W. Eisenstadt, M. Park, and H. Yu, "Silicon substrate coupling noise modeling, analysis, and experimental verification for mixed signal integrated circuit design," in *Microwave Symposium Digest, 2001 IEEE MTT-S International*, 2001, pp. 1727.

[83] S. Donnay and G. Gielen, *Substrate Noise Coupling in Mixed-Signal ASICs* vol. 1: Springer, 2003.

[84] X. Aragones, J. L. Gonzalez, and A. Rubio, *Analysis and solutions for switching noise coupling in mixed-signal ICs*: Kluwer Academic Pub, 1999.

[85] S. Masui, "Simulation of substrate coupling in mixed-signal MOS circuits," in *VLSI Circuits, 1992. Digest of Technical Papers., 1992 Symposium on*, 1992, pp. 42.

[86] W. S. Kwon, D. T. Alastair, K. H. Teo, S. Gao, T. Ueda, T. Ishigaki, K. T. Kang, and W. S. Yoo, "Stress evolution in surrounding silicon of Cu-filled through-silicon via undergoing thermal annealing by multiwavelength micro-Raman spectroscopy," *Applied Physics Letters,* vol. 98, p. 232106, 2011.

[87] A. M. Niknejad and R. G. Meyer, "Analysis of Eddy-Current Losses Over Conductive Substrates with Applications to Monolithic Inductors and Transformers," *IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES,* vol. 49, 2001.

[88] R. Gharpurey, "Modeling and analysis of substrate coupling in integrated circuits," Citeseer, 1995.

[89] R. Gharpurey and R. Meyer, "Modeling and analysis of substrate coupling in integrated circuits," in *Custom Integrated Circuits Conference, 1995., Proceedings of the IEEE 1995*, 1995, pp. 125.

[90] A. Niknejad, R. Gharpurey, and R. Meyer, "Numerically stable Green function for modeling and analysis of substrate coupling in integrated circuits," *IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS,* vol. 17, p. 305, 1998.

[91] J. Jackson and R. Fox, "Classical electrodynamics," *American Journal of Physics,* vol. 67, p. 841, 1999.

[92] G. Roach, *Green's functions*: Cambridge Univ Pr, 1982.

[93] Z. Ye, W. Yu, and Z. Yu, "Efficient 3-d capacitance extraction considering lossy substrate with multilayered green's function," *IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES,* vol. 54, pp. 2128, 2006.

[94] L. Cadix, A. Farcy, C. Bermond, C. Fuchs, P. Leduc, M. Rousseau, M. Assous, A. Valentian, J. Roullard, and E. Eid, "Modelling of through silicon via RF performance and impact on signal transmission in 3D integrated circuits," in *3D System Integration, 2009. 3DIC 2009. I EEE International Conference on*, ed San Francisco, CA: IEEE, 2009, pp. 1.

[95] L. Cadix, C. Bermond, C. Fuchs, A. Farcy, P. Leduc, L. DiCioccio, M. Assous, M. Rousseau, F. Lorut, and L. L. Chapelon, "RF characterization and modelling of high density Through Silicon Vias for 3D chip stacking," *Microelectronic Engineering,* vol. 87, pp. 491, 2010.

[96] Z. Zong, S. Mohammadzadeh, Y. Cao, Z. Qiu, R. Liu, R. Streiter, and T. Gessner, "Electrical resistivity calculations for copper nanointerconnect," *Microelectronic Engineering,* vol. 87, pp. 402, 2010.

[97] H.-S. Wong, L. Wei, and J. Deng, "The future of CMOS scaling-parasitics engineering and device footprint scaling," in *Solid-State and I ntegrated-Circuit Technology, 2008. ICSICT 2008. 9th International Conference on*, 2008, pp. 21.

[98] P. Dorsey, "Xilinx stacked silicon interconnect technology delivers breakthrough fpga capacity, bandwidth, and power efficiency," *Xilinx White Paper: Virtex-7 FPGAs,* pp. 1, 2010.

[99] Y. Xie and Y. Ma, "Design space exploration for 3D integrated circuits," in *Solid-State and Integrated-Circuit Technology, 2008. ICSICT 2008. 9th International Conference on*, 2008, pp. 2317.

[100] P. Schneider, S. Reitz, A. Wilde, G. Elst, and P. Schwarz, "Towards a methodology for analysis of interconnect structures for 3D-integration of micro systems," *Analog Integrated Circuits and Signal Processing,* vol. 57, pp. 205, 2008.

[101] L. W. Kong, J. R. Lloyd, K. B. Yeap, E. Zschech, A. Rudack, M. Liehr, and A. Diebold, "Applying x-ray microscopy and finite element modeling to identify the mechanism of stress-assisted void growth in through-silicon vias," *Journal of Applied Physics,* vol. 110, p. 053502, 2011.

[102] C. Christopoulos, *The transmission-line modeling method: TLM*: IEEE Piscataway NJ, 1995.

[103] C. Christopoulos, I. o. Electrical, and E. Engineers, "The transmission-line modeling method: TLM," 1995.

[104] COMSOL, "http://www.comsol.com."

[105] T. Vucurevich, "The Long Road to 3-D Integration: Are We There Yet," in *Keynote speech at the 3D Architecture Conference*, 2007.

[106] R. N. Bracewell and R. Bracewell, *The Fourier transform and i ts applications* vol. 31999: McGraw-Hill New York, 1986.

[107] W. Burger and M. J. Burge, *Digital image processing*: Springer, 2008.

[108] C. P. Wen, "Coplanar waveguide: A surface strip transmission line suitable for nonreciprocal gyromagnetic device applications," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 17, pp. 1087, 1969.

[109] D. A. Frickey, "Conversions between S, Z, Y, H, ABCD, and T parameters which are valid for complex source and load impedances," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 42, pp. 205, 1994.

[110] J. Everard, "Two Port Network Parameters," *Fundamentals of RF Circuit Design: with Low Noise Oscillators,* pp. 63.

[111] T. Belytschko, Y. Y. Lu, and L. Gu, "Element‐free Galerkin methods," *International journal for numerical methods in engineering,* vol. 37, pp. 229, 1994.

[112] S. Ghosh, *Network Theory: Analysis and Synthesis*201: PHI Learning Pvt. Ltd., 2005.

[113] F. Fang, M. Franke, D. Gaebler, and K. S. Sool, "PIN photodiode bandwidth optimization in integrated CMOS process," in *SPIE Optics+ Optoelectronics*, 2011, pp. 80732E.

[114] R. J. Baker, *CMOS: circuit design, layout, and simulation* vol. 18: Wiley-IEEE Press, 2011.

[115] M. Abouelatta-Ebrahim, C. Gontrand, and A. Zekry, "Design of complementary LDMOS in 0.35 μm BiCMOS technology for smart integration," *The European Physical Journal Applied Physics,* vol. 57, p. 10103, 2011.

[116] V. Leus and D. Elata, "Fringing field effect in electrostatic actuators," *Technion–Israel Institute of Technology,* pp. 2004, 2004.

[117] K. Pillai, "Fringing field of finite parallel-plate capacitors," in *Proceedings of the Institution of Electrical Engineers*, 1970, pp. 1201.

[118] S.-h. GE and F.-h. ZHAI, ZHAI, "The Exact Solution of Capacitance for Long Square Cylinder Capacitors," *Journal of Qingdao University of Science and Technology,* vol. 24, p. 466, 2003.

[119] H. Lawrence and R. Warner Jr, "Diffused junction depletion layer calculations," *Bell Syst. Tech. J,* vol. 39, pp. 389, 1960.

[120] H. Gummel and D. Scharfetter, "Depletion‐Layer Capacitance of p+ n Step Junctions," *Journal of Applied Physics,* vol. 38, pp. 2148, 1967.

[121] R. F. Pierret, *Semiconductor device fundamentals*: Pearson Education India, 1996.

[122] R. Gharpurey and R. G. Meyer, "Modeling and analysis of substrate coupling in integrated circuits," *Solid-State Circuits, IEEE Journal of,* vol. 31, pp. 344, 1996.

[123] C. Xu, R. Gharpurey, T. S. Fiez, and K. Mayaram, "A green function-based parasitic extraction method for inhomogeneous substrate layers," in *Proceedings of the 42nd annual Design Automation Conference*, 2005, pp. 141.

[124] L. M. Silveira and N. Vargas, "Characterizing substrate coupling in deep-submicron designs," *Design & Test of Computers, IEEE,* vol. 19, pp. 4, 2002.

[125] E. Charbon, R. Gharpurey, P. Miliozzi, R. G. Meyer, and A. L. Sangiovanni-Vincentelli, *Substrate noise: analysis and optimization for IC design*: Springer, 2001.

[126] J.-E. Lorival, F. SUN, F. Frantz, F. Calmon, M. Le Berre, I. O'Connor, O. Valorge, C. Fuchs, J. Charbonnier, and C. Gontrand, "Efficient and Simple Compact Modeling Approach for 3-D Interconnects with IC's Stack Global Electrical Context Consideration," unpublished.

[127] E. B. Rosa, *The self and mutual inductances of linear conductors*: US Department of Commerce and Labor, Bureau of Standards, 1908.

[128] J. Nurmi, J. Isoaho, H. Tenhunen, and A. Jantsch, *Interconnect-centric design for advanced SoC and NoC*: Springer Science+ Business Media, 2004.

[129] C. Fuchs, "3D-TSV Integration for Multi-Media and Mobile applications," in *EUROPEAN NANOELECTRONICS FORUM*, Madrid, 2010.

[130] T. Smedes, N. Van Der Meijs, and A. Van Genderen, "Extraction of circuit models for substrate cross-talk," in *Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design*, 1995, pp. 199.

[131] F. SUN, J.-E. Lorival, F. Calmon, and C. Gontrand, "Through Silicon Vias: from a physical point of view to compact models," unpublished.

[132] O. Valorge, F. SUN, J.-E. Lorival, M. Abouelatta-Ebrahim, F. Calmon, and C. Gontrand, "Analytical and Numerical Model Confrontation for Transfer Impedance Extraction in Three-Dimensional Radio Frequency Circuits," *Circuits and Systems,* vol. 3, pp. 126, 2012.

[133] *Matlab*. Available: http://mathworks.com

[134] *Advanced Design System ADS 2009*. Available: http://www.home.agilent.com.

[135] S. Cheramy, J. Charbonnier, D. Henry, A. Astier, P. Chausse, M. Neyret, C. Brunet-Manquat, S. Verrun, N. Sillon, and L. Bonnot, "3D integration process flow for set-top box application: description of technology and electrical results," in *Microelectronics and Packaging Conference, 2009. EMPC 2009. European*, 2009, pp. 1.

[136] G. F. Engen and C. A. Hoer, "Thru-reflect-line: An improved technique for calibrating the dual six-port automatic network analyzer," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 27, pp. 987, 1979.

[137] H. Zhao, A.-Y. Tang, P. Sobis, T. Bryllert, K. Yhland, J. Stenarson, and J. Stake, "VNA-calibration and S-parameter characterization of submillimeter wave integrated membrane circuits," in *Infrared Millimeter and T erahertz Waves (IRMMW-THz), 2010 35th International Conference on*, 2010, pp. 1.

[138] A. P. Ferrero and U. Pisani, "Two-port network analyzer calibration using an unknown'thru'," *IEEE Microwave and Guided Wave Letters,* vol. 2, pp. 505, 1992.

[139] H.-J. Eul and B. Schiek, "Thru-match-reflect: One result of a rigorous theory for de-embedding and network analyzer calibration," in *Microwave Conference, 1988. 18th European*, 1988, pp. 909.

[140] A. E. EDA. *De-embedding techniques in advanced design system*. Available: http://cp.literature.agilent.com/litweb/pdf/5989-9451EN.pdf

[141] COMSOL, *RF Module User's Guide*: COMSOL Multiphysics, 2010.

[142] J.-M. Jin and J. Jin, *The finite element method in electromagnetics*: Wiley New York, 2002.

[143] COMSOL. (2010). *User's Guide*.

[144] D. Mattis and J. Bardeen, "Theory of the anomalous skin effect in normal and superconducting metals," *Physical Review,* vol. 111, p. 412, 1958.

[145] A. He, T. Osborn, S. A. B. Allen, and P. A. Kohl, "All-Copper Chip-to-Substrate Interconnects Part II. Modeling and Design," *Journal of the Electrochemical Society,* vol. 155, pp. D314, 2008.

[146] G. Katti, A. Mercha, M. Stucchi, Z. Tokei, D. Velenis, J. Van Olmen, C. Huyghebaert, A. Jourdain, M. Rakowski, I. Debusschere, P. Soussan, H. Oprins, W.

Dehaene, K. De Meyer, Y. Travaly, E. Beyne, S. Biesemans, and B. Swinnen, "Temperature dependent electrical characteristics of through-si-via (TSV) interconnections," in *Interconnect Technology Conference (IITC), 2010 International*, 2010, pp. 1.

[147] S. H. Pan, N. Chang, and J. Zheng, "IC-Package Thermal Co-Analysis in 3D IC Environment," 2011.

[148] Y. Zhan, B. Goplen, and S. S. Sapatnekar, "Electrothermal analysis and optimization techniques for nanoscale integrated circuits," in *Proceedings of the 2006 Asia and South Pacific Design Automation Conference*, 2006, pp. 219.

[149] Y. Zhan and S. S. Sapatnekar, "High-efficiency Green function-based thermal simulation algorithms," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on,* vol. 26, pp. 1661, 2007.

[150] W.-Y. Yin, K. Kang, and J.-F. Mao, "Electromagnetic-thermal characterization of on on-chip coupled (a) symmetrical interconnects," *Advanced Packaging, IEEE Transactions on,* vol. 30, pp. 851, 2007.

[151] Y. Zhou, G. Xiao, and J. Mao, "Generalized heat transition matrix for multi-domain electro-thermal analysis," in *Microwave Conference Proceedings (APMC), 2010 Asia-Pacific*, 2010, pp. 2164.

[152] J.-C. Krencker, J.-B. Kammerer, Y. Herve, and L. Hebrard, "Electro-thermal high-level modeling of integrated circuits," in *Thermal Investigations of ICs and Systems (THERMINIC), 2012 18th International Workshop on*, 2012, pp. 1.

[153] S. Kim and D. Neikirk, "Compact equivalent circuit model for the skin effect," in *Microwave Symposium Digest, 1996., IEEE MTT-S International*, 1996, pp. 1815.

[154] J. Cho, E. Song, K. Yoon, J. S. Pak, J. Kim, W. Lee, T. Song, K. Kim, J. Lee, and H. Lee, "Modeling and analysis of through-silicon via (TSV) noise coupling and suppression using a guard ring," *Components, Packaging and M anufacturing Technology, IEEE Transactions on,* vol. 1, pp. 220, 2011.

[155] J. Kim, J. S. Pak, J. Cho, E. Song, J. Cho, H. Kim, T. Song, J. Lee, H. Lee, and K. Park, "High-frequency scalable electrical model and analysis of a through silicon via (TSV)," *Components, Packaging and Manufacturing Technology, IEEE Transactions on,* vol. 1, pp. 181, 2011.

[156] A. Weisshaar, H. Lan, and A. Luoh, "Accurate closed-form expressions for the frequency-dependent line parameters of on-chip interconnects on lossy silicon substrate," *Advanced Packaging, IEEE Transactions on,* vol. 25, pp. 288, 2002.

[157] A. Van der Ziel, "Noise. Sources, characterization, measurement," *Prentice-Hall Information and System Sciences Series, Englewood Cliffs: Prentice-Hall, 1970,* vol. 1, 1970.

[158] K. Van Vliet, A. Friedmann, R. Zijlstra, A. Gisolf, and A. Van der Ziel, "Noise in single injection diodes. I. A survey of methods," *Journal of Applied Physics,* vol. 46, pp. 1804, 1975.

[159] K. Van Vliet, A. Friedmann, R. Zijlstra, A. Gisolf, and A. Van der Ziel, "Noise in single injection diodes. II. Applications," *Journal of Applied Physics,* vol. 46, pp. 1814, 1975.

[160] J. B. Johnson, "The Schottky effect in low frequency circuits," *Physical Review,* vol. 26, p. 71, 1925.

[161] W. H. Press, "Flicker noises in astronomy and elsewhere," *Comments on Astrophysics,* vol. 7, pp. 103, 1978.

[162] R. Rammal, C. Tannous, P. Breton, and A.-M. Tremblay, "Flicker (1/f) noise in percolation networks: A new hierarchy of exponents," *Physical review letters,* vol. 54, pp. 1718, 1985.

[163] A. Topol, D. L. Tulipe, L. Shi, D. Frank, K. Bernstein, S. Steen, A. Kumar, G. Singco, A. Young, and K. Guarini, "Three-dimensional integrated circuits," *IBM Journal of Research and Development,* vol. 50, pp. 491, 2006.

[164] Teraflops. Available: http://www.intel.com/pressroom/kits/teraflops/

[165] U. Kang, H.-J. Chung, S. Heo, S.-H. Ahn, H. Lee, S.-H. Cha, J. Ahn, D. Kwon, J. H. Kim, and J.-W. Lee, "8Gb 3D DDR3 DRAM using through-silicon-via technology," in *Solid-State Circuits Conference-Digest of Technical Papers, 2009. ISSCC 2009. IEEE International*, 2009, pp. 130.

[166] Tezzaron. Available: http://www.tezzaron.com/

[167] R. Gharpurey, "Modeling and Analysis of Substrate Coupling in Integrated Circuits," Engineering-Electrical Engineering and Computer Sciences, University of California, Berkeley, 1992.

[168] J. R. Mosig and T. K. Sarkar, "Comparison of quasi-static and exact electromagnetic fields from a horizontal electric dipole above a lossy dielectric backed by an imperfect ground plane," *Microwave Theory and T echniques, IEEE Transactions on,* vol. 34, pp. 379, 1986.

List of personal publications

Journal

[1] Olivier VALORGE, *Fengyuan SUN*, Jean-etienne LORIVAL, Mohamed ABOUELATTA-EBRAHIM, Francis CALMON, and Christian GONTRAND, "Analytical and Numerical Model Confrontation for Transfer Impedance Extraction in Three-Dimensional Radio Frequency Circuits," *Circuits and Systems*, vol. 3, pp. 126, 2012.

[2] Rabah DAHMANI, Olivier VALORGE, *Fengyuan SUN*, Samir LABIOD, Francis CALMON, Sa DA LATRECHE, Ian O'CONNOR, and CHRISTIAN GONTRAND, "Insights into Three-Dimensional Radiofrequency Circuits Connections," *Computer Technology and Application,* vol. 2, pp. 456, 2011.

[3] Christian GONTRAND, Olivier VALORGE, Rabah DAHMANI, *Fengyuan SUN*, Francis CALMON, Jacques VERDIER, and Paul DAUTRICHE, "Some Tools to Model Ground or Supply Bounces Induced in and out of Heterogeneous Integrated Circuits," *Computer Technology and A pplication*, vol. 2, pp. 33, 2011.

[4] *Fengyuan SUN*, Jean-etienne LORIVAL, Francis CALMON, and Christian GONTRAND, "Through Silicon Vias: from a physical point of view to compact models," *COMPEL: The International Journal for Computation and Mathematics in Electrical and Electronic Engineering* ***(Accepted)***

[5] *Fengyuan SUN*, Jean-etienne LORIVAL, Olivier VALORGE, Francis CALMON, and Christian GONTRAND, "Transmission Line Method, Green kernels, Transfer impedance: Some Analog Ways to Analyse Substrate and Connectics Entanglement in Three-Dimensional Radiofrequency Circuits," submitted to *Microelectronics Reliability*.

[6] Jean-etienne LORIVAL, *Fengyuan SUN*, Felipe FRANTZ, Francis CALMON, Martine LE BERRE, Ian O'CONNOR, Olivier VALORGE, Christine FUCHS, Jean CHARBONNIER, and Christian GONTRAND, "Efficient and Simple Compact Modeling Approach for 3-D Interconnects with IC's Stack Global Electrical Context Consideration," submitted to *IEEE, Transaction on Circuits and Systems* .

[7] Christian GONTRAND, *Fengyuan SUN*, Francis CALMON, and Jacques VERDIER, "Towards Signal fluctuations Correlation Analysis via a Transfer Impedance Approach into Three-Dimensional Radiofrequency Analog Circuits," submitted to *Microelectronics Journal*.

International Conference

[1] *Fengyuan SUN*, Jean-etienne LORIVAL, Francis CALMON, and Christian GONTRAND, "Physically Based Approach of Simple Compact Modeling for 3D Interconnect into RF circuits," in *Design, Automation & Test in Europe (DATE), W5.5*, Grenoble, 18-22 March 2013.

National Conference

[1] Jean-etienne LORIVAL, *Fengyuan SUN*, Francis CALMON, Christian GONTRAND, and Ian O'CONNOR, "Through Silicon Vias (TSV) Modeling for 3-D Integration Approach Overview and Presentation of 3D-TLE, a 3-D Extraction Tool," in *Journées Electroniques 2011*, Campus Saint-Priest, Université Montpellier II, Montpellier,France, 27-28 october, 2011.

[2] *Fengyuan SUN*, Jean-etienne LORIVAL, Francis CALMON, and Christian GONTRAND, "Physically Based Approach of Simple Compact Modeling for 3D Interconnect into RF circuits," in *GDR SOC-SIP* , Lyon, 10-12 June 2013.